ELECTRICAL REF DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QTY
C1,2,11,20,95,	1	702W07301	CAP., 20, 15V	8
112,171,181				
C3 THRU 10,	2	702W07818	CAP., 0.1, 50V	181
12 THRU 19,				
21 THRU 94,				
96 THRU 111,				
113 THRU 170,				
172 THRU 180,				
182 THRU 189				
F1	3	708W11402	FUSE, 10 AMP	1
R1 THRU 7,9,	4	703W27888	RES, 15 OHMS	71
13 THRU 19,22,				
24 THRU 31,34,				
36 THRU 42,44,45,				
48 THRU 55,57,				
60 THRU 63,				
65 THRU 69,				
72 THRU 78,81,82,				
85,88 THRU 96				
R8,10,11,20,21,	5	703W27488	RES, 10 OHMS	24
23,32,33,35,43,				
46,47,56,58,59,				
64,70,71,79,80,				
83,84,86,87				
R12,113,129,132	6	703W32288	RES, 1K OHMS	4
R97 THRU 112,128	7	703W28488	RES, 27 OHMS	17
R114,	8	703P10005	RES, ZERO OHMS	12
117 THRU 124,				
126,130,134				
R136 THRU 145	9	703W30688	RES, 220 OHMS	10
U1 THRU 4,	10	703W01562	IC, MK4164	68
9 THRU 12,				
17 THRU 20,				
25 THRU 28,				
34 THRU 37,				

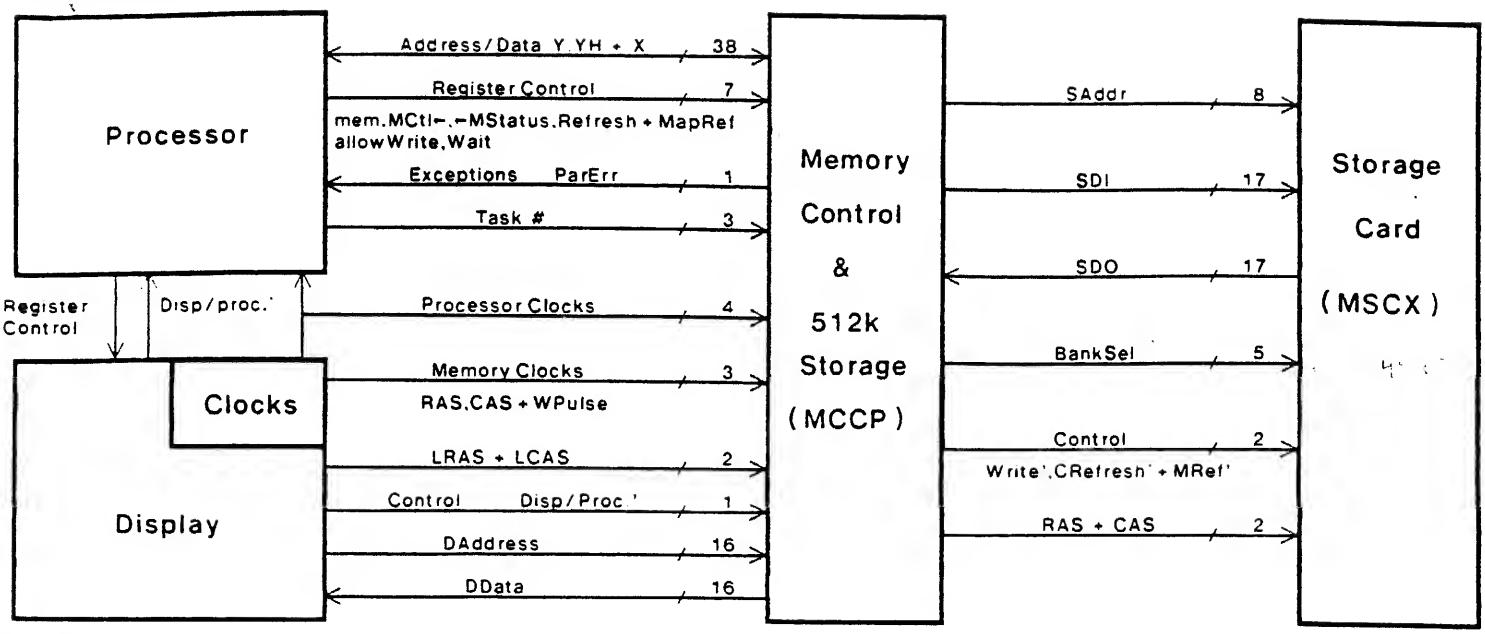
TITLE	DWG. SIZE	DWG. NO.	SHEET REV
PWB ASSY, MCC-P (256K)	A4	140S05950	A
		SHEET 1 OF 3	

ELECTRICAL REF DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QTY
42 THRU 45,				
51 THRU 54,				
60 THRU 63,				
68 THRU 71,				
77 THRU 80,				
86 THRU 89,				
94 THRU 97,				
103 THRU 106,				
111 THRU 114,				
120 THRU 123,				
129 THRU 132,				
137 THRU 140				
U33,85,102	11	703W13291	IC, 1KX15	3
U50,59,76,119,	12	733W01634	IC, SN74S241	9
128,145,165,211,				
212				
U146 THRU 154,	13	733W01633	IC, SN74S240	16
156,158,164,182,				
200,202,207				
U155,157	14	733W02136	IC, SN74S37	2
U159,166,179,203	15	733W01638	IC, SN74S280	4
U172,183,192	16	733W01616	IC, SN74S138	3
U161	17	733W01635	IC, SN74S251	1
U162,163,171,177,	18	733W00318	IC, SN74S00	6
184,209				
U167,213	19	733W01606	IC, SN74S10	2
U168	20	733W01648	IC, SN74S86	1
U169,185,193	21	733W01771	IC, SN74S74	3
U170,194,201	22	733W01643	IC, SN74S02	3
U174	23	733W01663	IC, SN74LS393	1
U175,208	24	733W01640	IC, SN74S374	2
U176,210	25	733W00319	IC, SN74S04	2
U178,186	26	744W00001	IC, DELAY LINE	2
U180,181,188,189,	27	733W01636	IC, AM74S253	8
196,197,204,205				

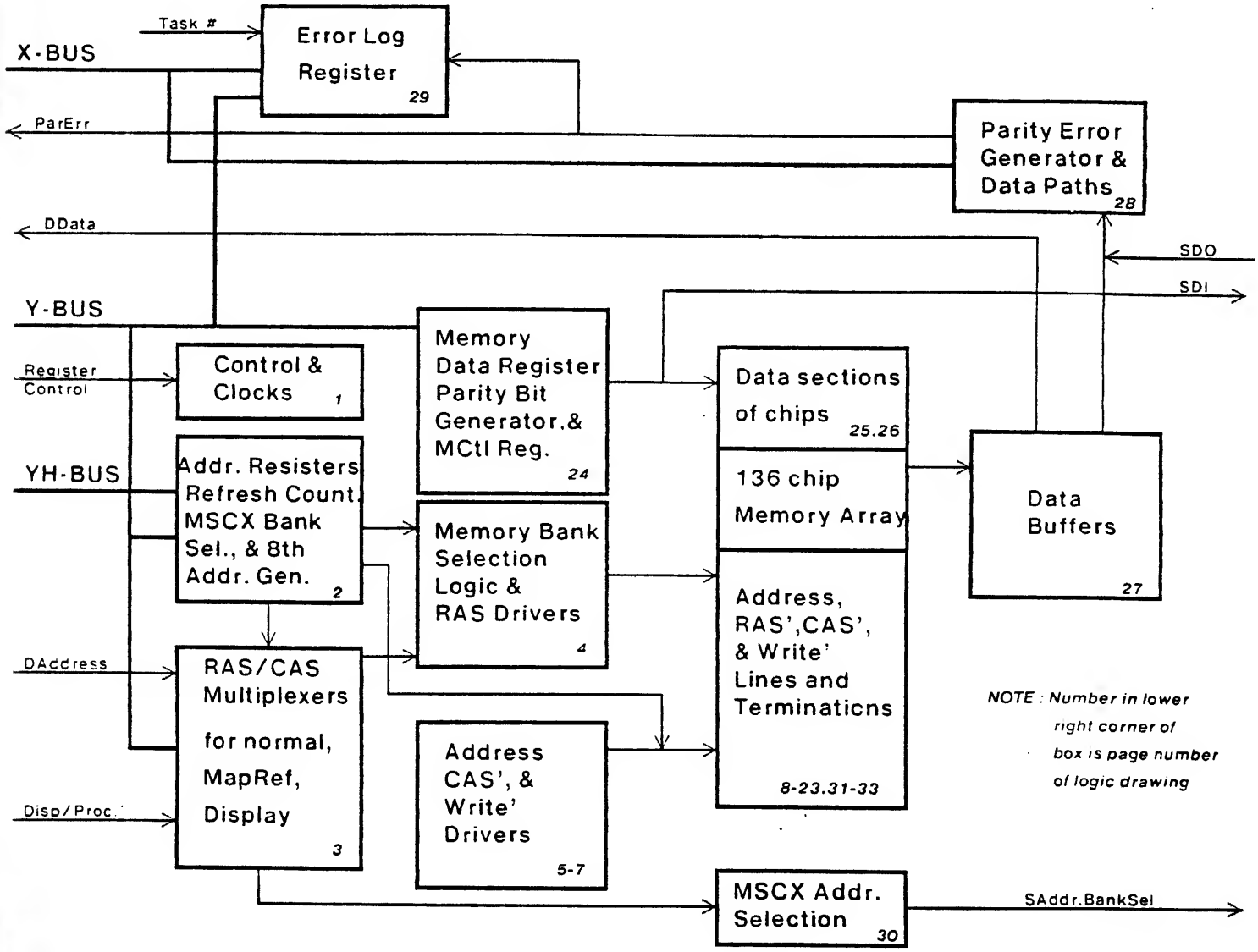
TITLE	DWG. SIZE	DWG. NO.	SHEET REV
PWB ASSY, MCC-P (256K)	A4	140S05950	A
		SHEET 2 OF 3	

TABLE OF CONTENTS

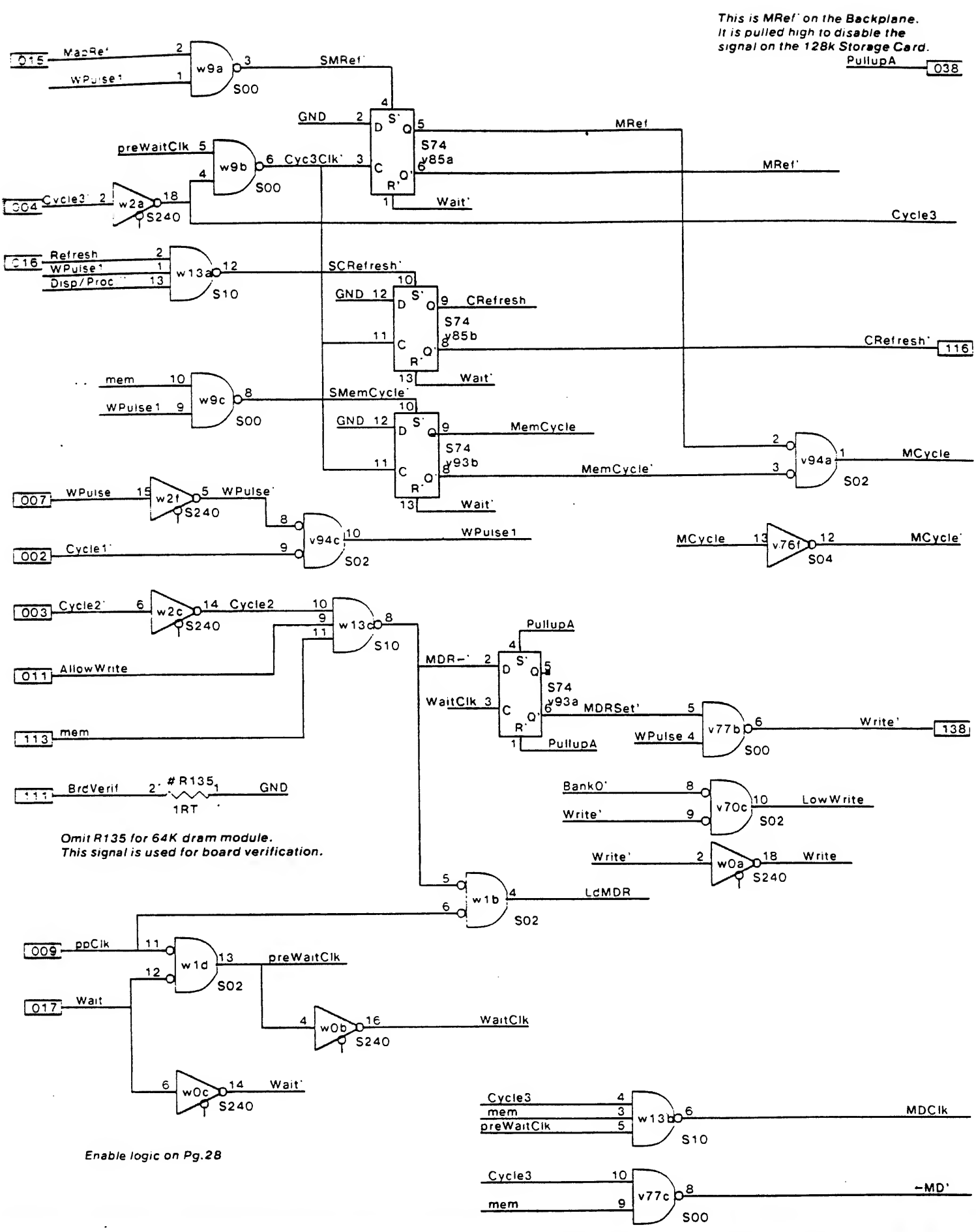
MEMORY SYSTEM



MCCP Block Diagram

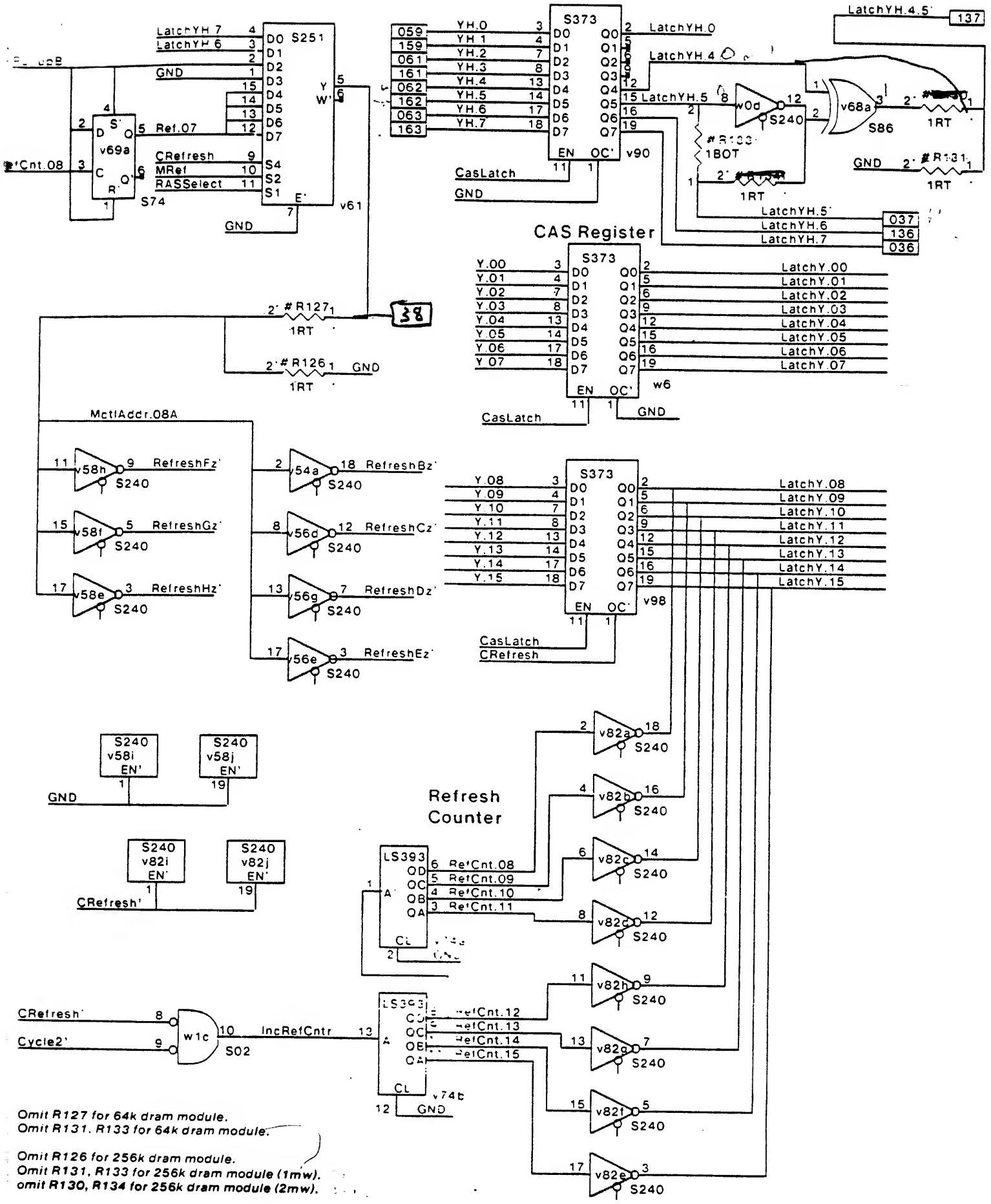


XEROX ED	Project	Reference	File	Designer	Rev	Date	Page
	MCCP	Memory Controller Block Diagram	PMCCP-0.4.sily	S. Ando	A	10/25/83	0.4



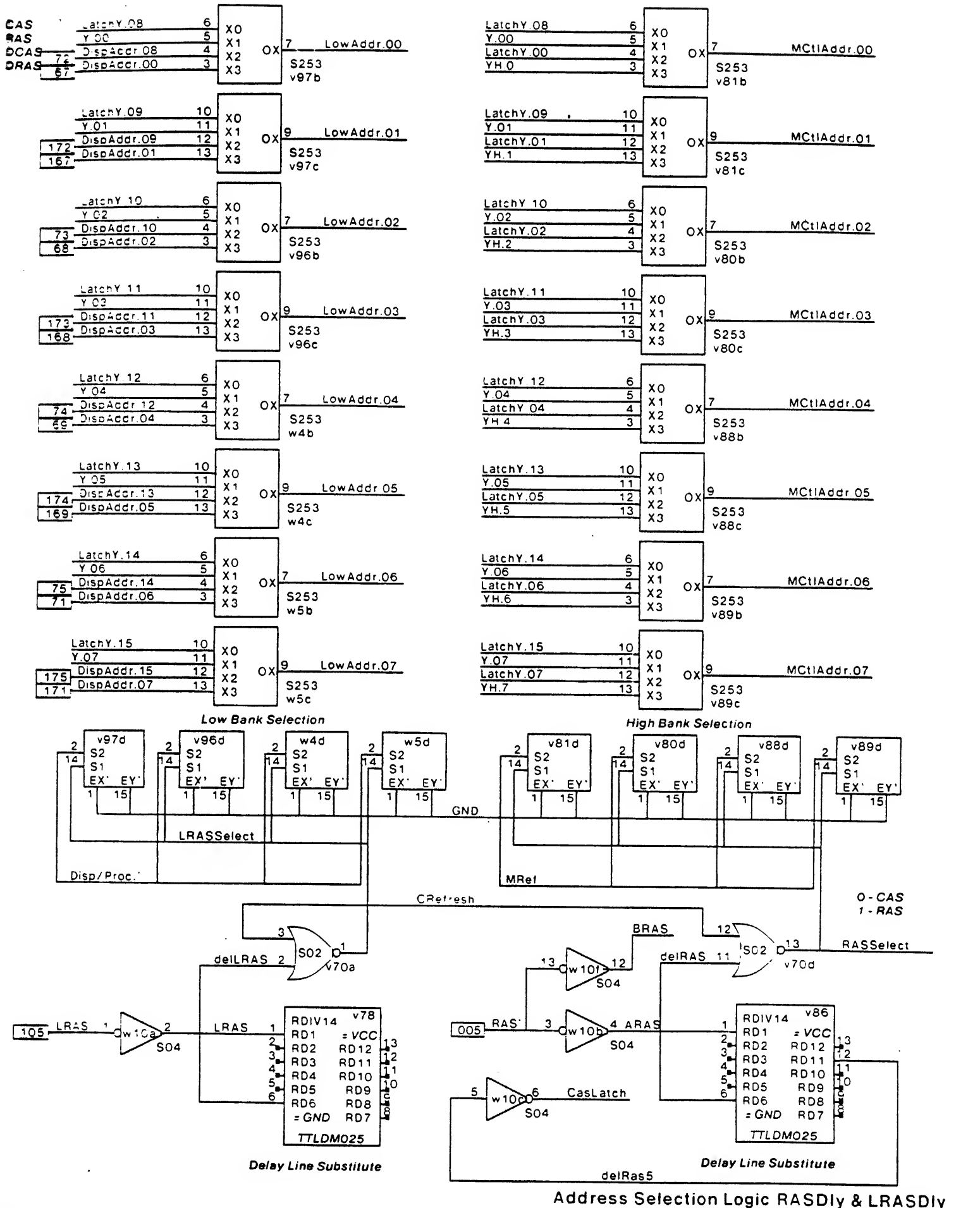
Write,CRefresh',MRef,LdMDR, CycleRcv. MDClk,-MD'

XEROX ED	Project MCCP	Write,CRefresh',MRef.LdMDR, CycleRcv. MDClk,-MD'	File PMCCP01.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 1

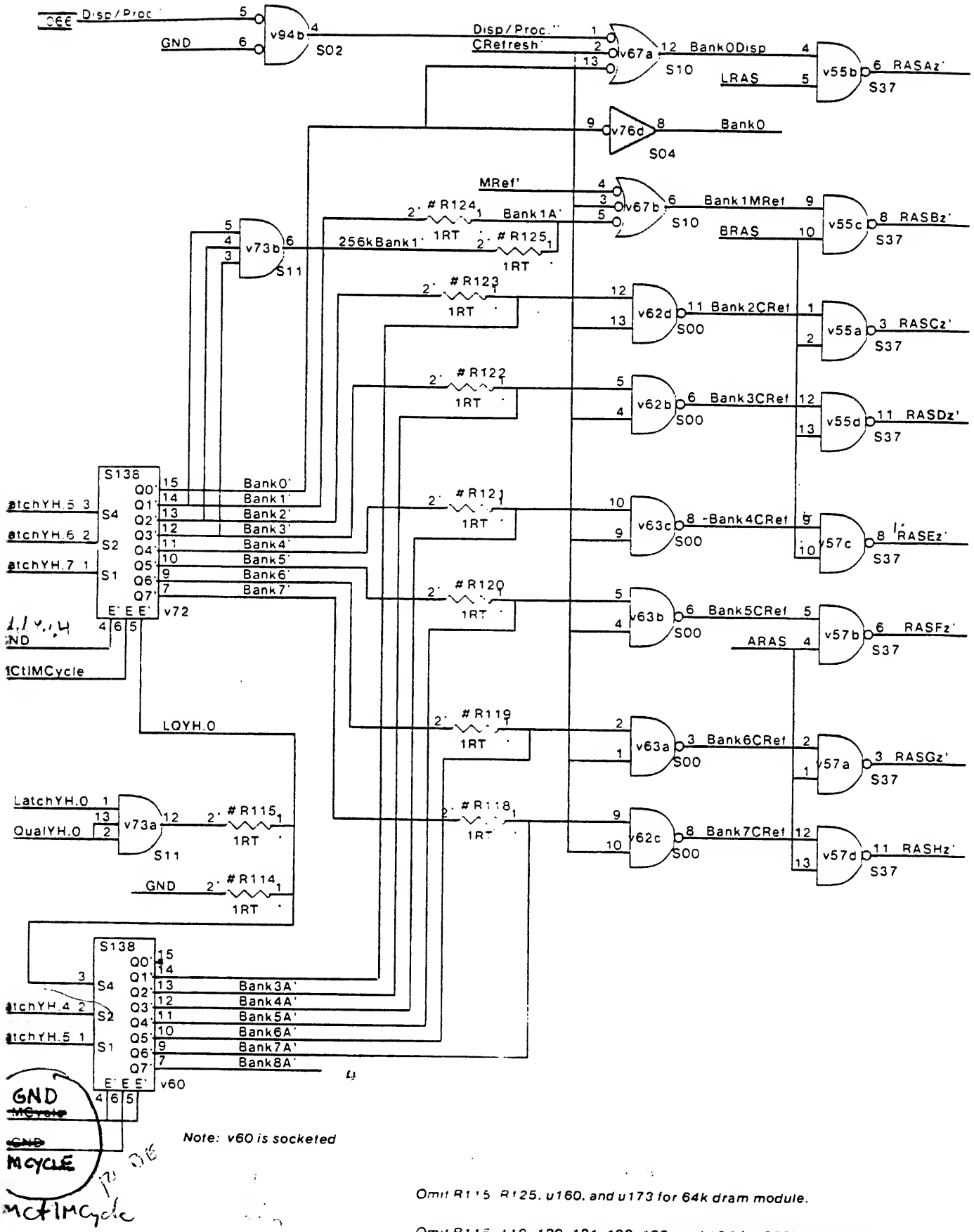


Address Selection, Refresh Counter & CAS Resisters

XEROX ED	Project MCCP	Addr. Select., Refresh Count. & CAS Resisters	File PMCCP02.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 2



XEROX ED	Project MCCP	Address Selection Logic RASDly & LRASDly	File PMCCP03.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 3



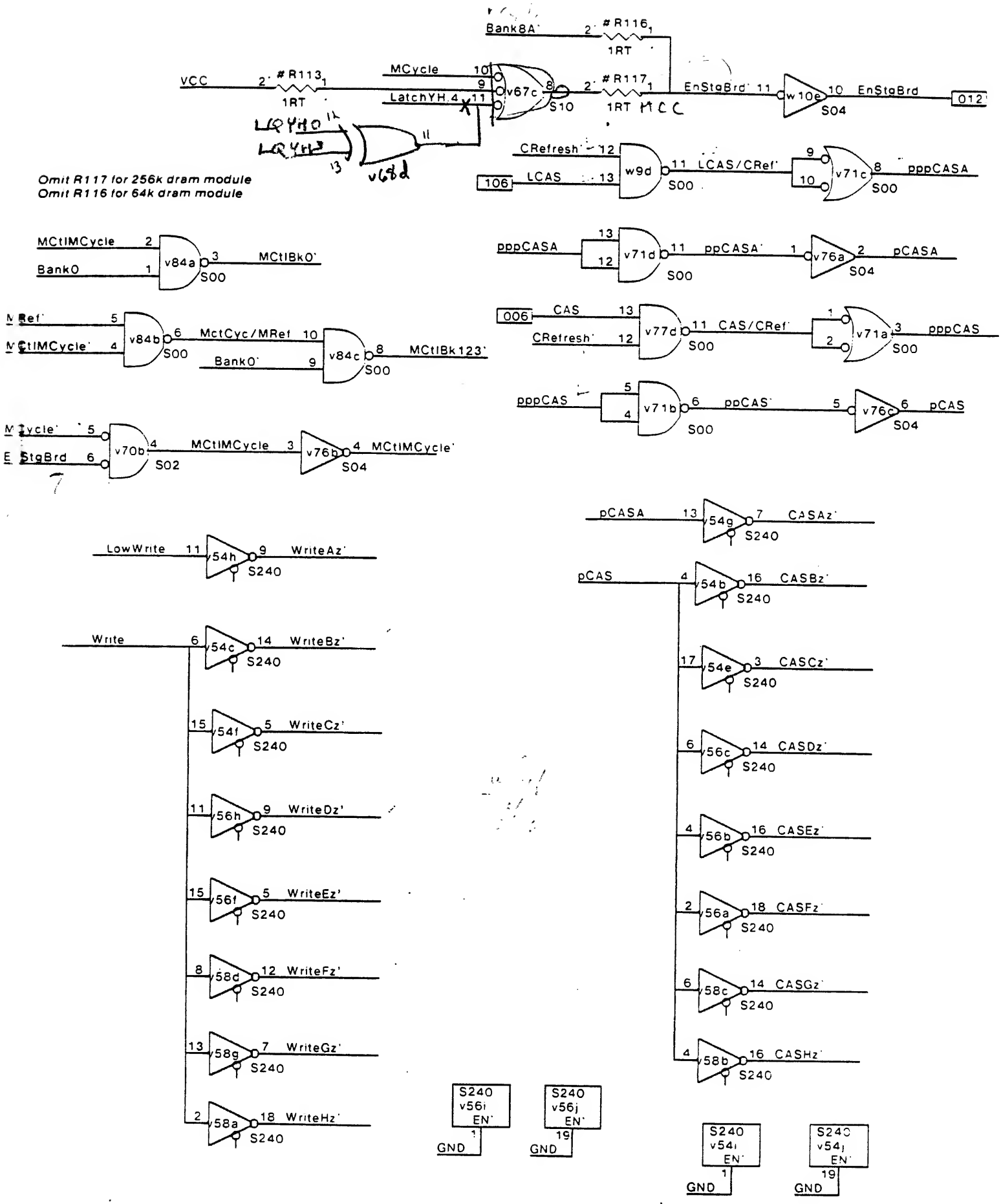
Note: v60 is socketed

Omit R115, R125, u160, and u173 for 64k dram module.

Omit R118, 119, 120, 121, 122, 123, and 124 for 256k dram module.
Omit R115 for 256k dram module (1 mw).
Omit R114 for 256k dram module (2 mw).

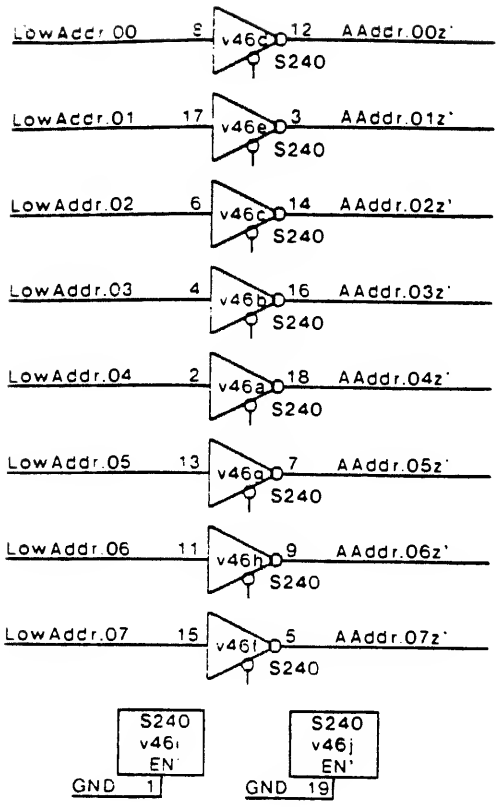
Memory Bank Selection

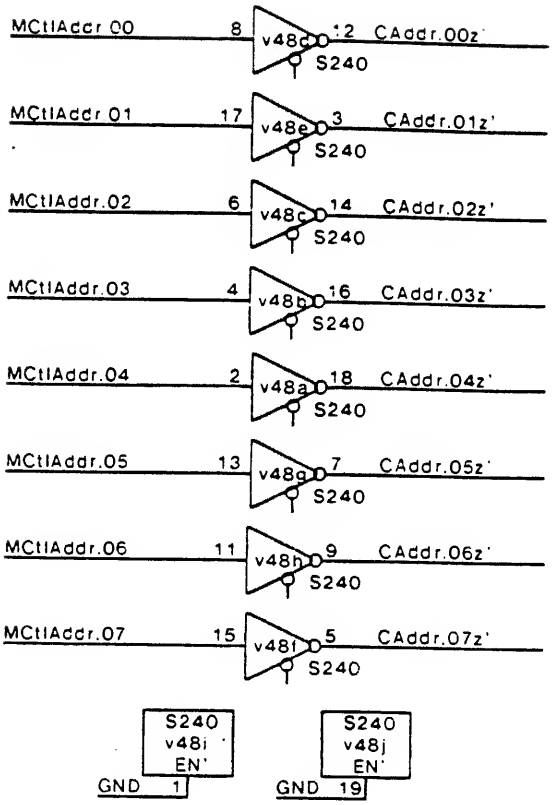
XEROX ED	Project MCCP	Memory Bank Selection	File PMCCP04.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 4

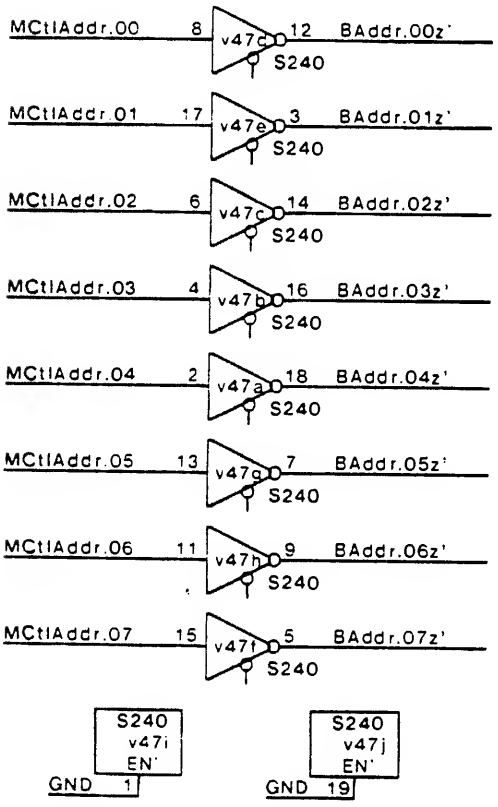


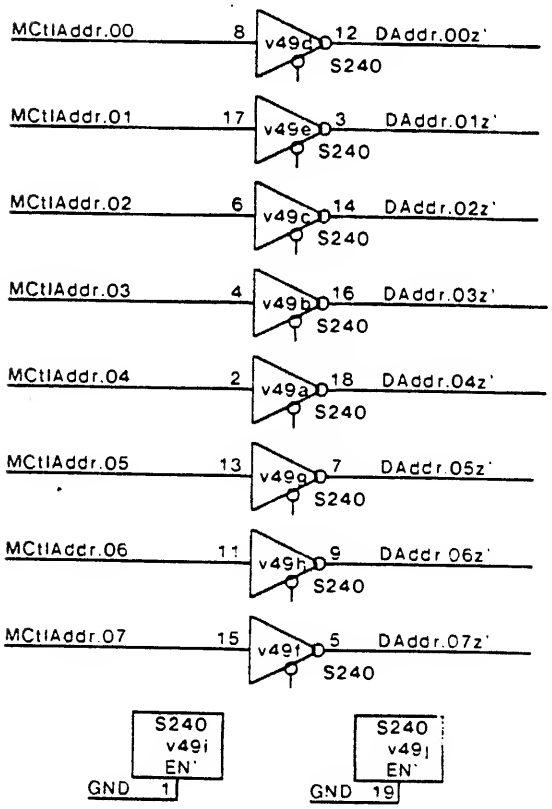
Memory Bank Selection/ Drivers for Write' and CAS'

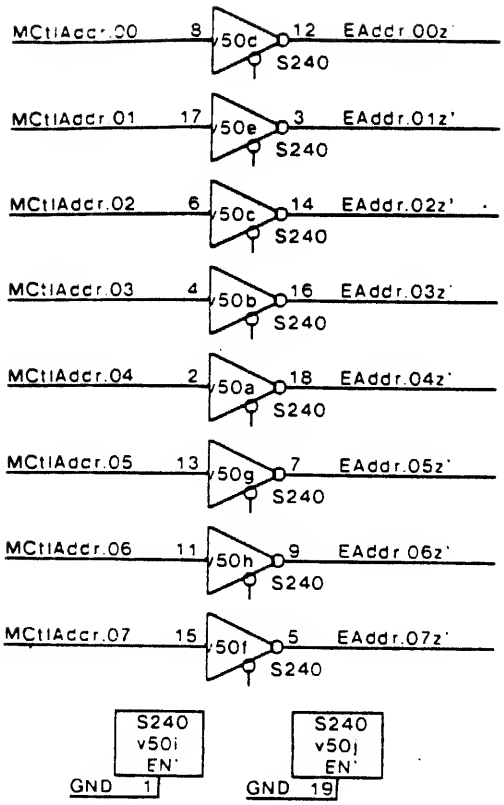
XEROX ED	Project MCCP	Memory Bank Selection Drivers for Write' & CAS'	File PMCCP05.sil	Designer S. Ando	Rev A	Date 10/17/83	Page 5

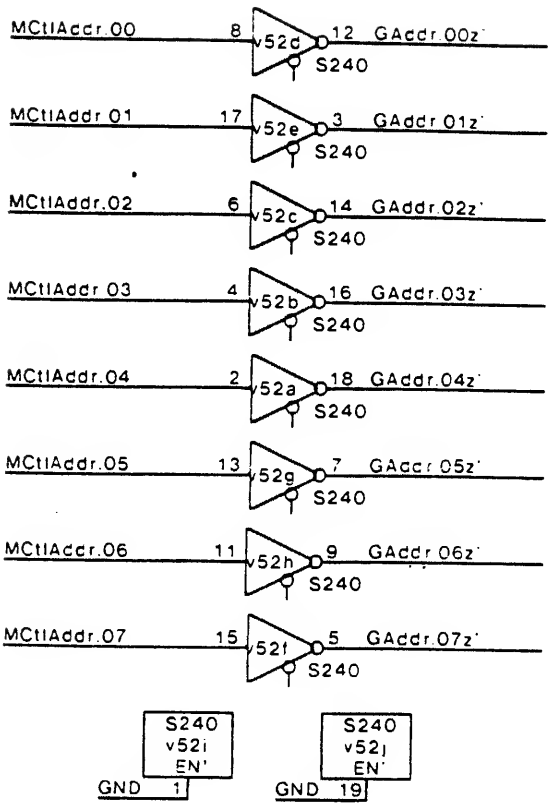

LowAddr.00 8 v46c 12 AAddr.00z'
LowAddr.01 17 v46e 3 AAddr.01z'
LowAddr.02 6 v46c 14 AAddr.02z'
LowAddr.03 4 v46b 16 AAddr.03z'
LowAddr.04 2 v46a 18 AAddr.04z'
LowAddr.05 13 v46g 7 AAddr.05z'
LowAddr.06 11 v46h 9 AAddr.06z'
LowAddr.07 15 v46f 5 AAddr.07z'
S240
S240 v46i EN' GND 1
S240 v46j EN' GND 19

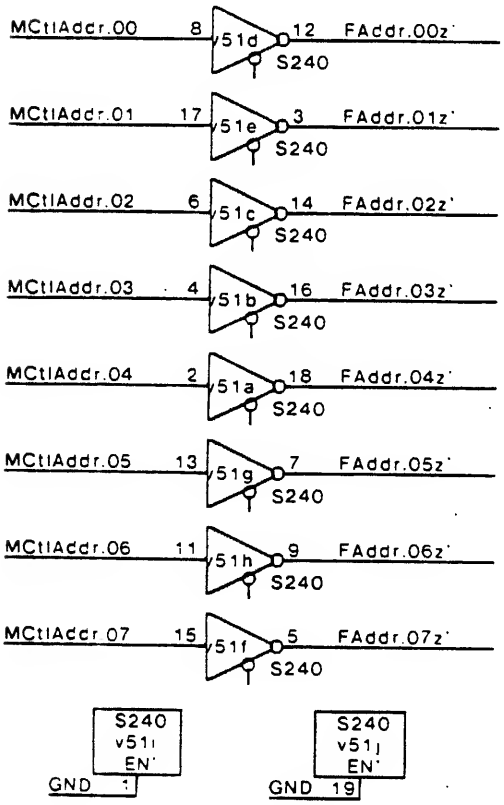

MCtlAddr.00 8 v48c 12 CAddr.00z'
MCtlAddr.01 17 v48e 3 CAddr.01z'
MCtlAddr.02 6 v48c 14 CAddr.02z'
MCtlAddr.03 4 v48b 16 CAddr.03z'
MCtlAddr.04 2 v48a 18 CAddr.04z'
MCtlAddr.05 13 v48g 7 CAddr.05z'
MCtlAddr.06 11 v48h 9 CAddr.06z'
MCtlAddr.07 15 v48f 5 CAddr.07z'
S240
S240 v48i EN' GND 1
S240 v48j EN' GND 19

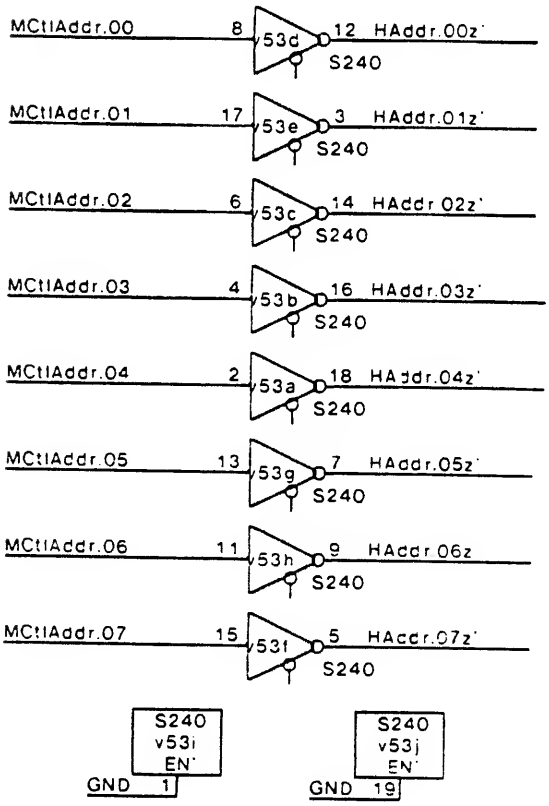

MCtlAddr.00 8 v47c 12 BAddr.00z'
MCtlAddr.01 17 v47e 3 BAddr.01z'
MCtlAddr.02 6 v47c 14 BAddr.02z'
MCtlAddr.03 4 v47b 16 BAddr.03z'
MCtlAddr.04 2 v47a 18 BAddr.04z'
MCtlAddr.05 13 v47g 7 BAddr.05z'
MCtlAddr.06 11 v47h 9 BAddr.06z'
MCtlAddr.07 15 v47f 5 BAddr.07z'
S240
S240 v47i EN' GND 1
S240 v47j EN' GND 19


MCtlAddr.00 8 v49c 12 DAddr.00z'
MCtlAddr.01 17 v49e 3 DAddr.01z'
MCtlAddr.02 6 v49c 14 DAddr.02z'
MCtlAddr.03 4 v49b 16 DAddr.03z'
MCtlAddr.04 2 v49a 18 DAddr.04z'
MCtlAddr.05 13 v49g 7 DAddr.05z'
MCtlAddr.06 11 v49h 9 DAddr.06z'
MCtlAddr.07 15 v49f 5 DAddr.07z'
S240
S240 v49i EN' GND 1
S240 v49j EN' GND 19



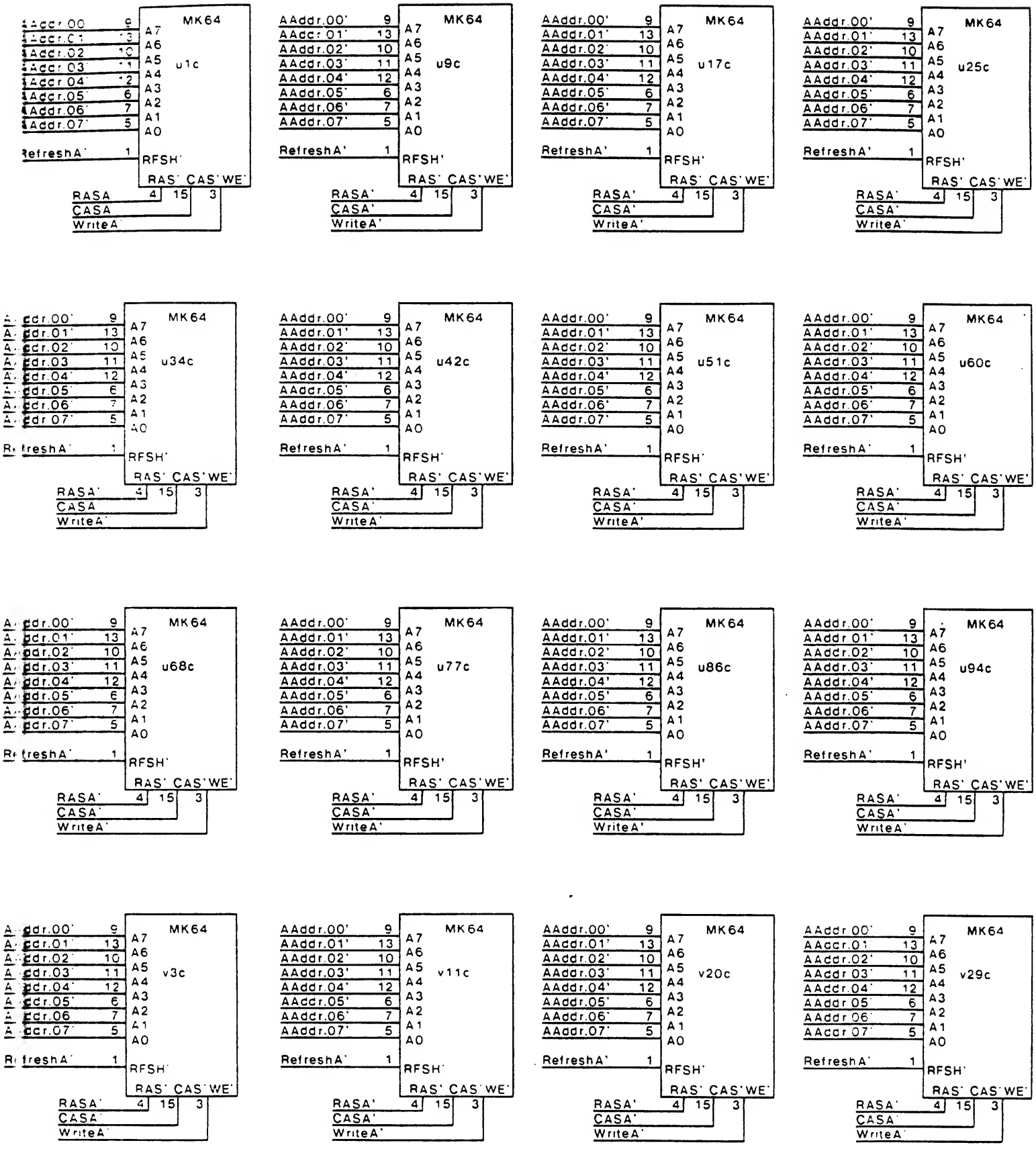






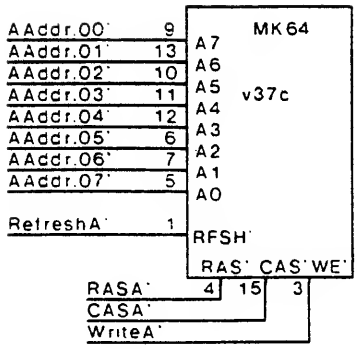
Address Drivers

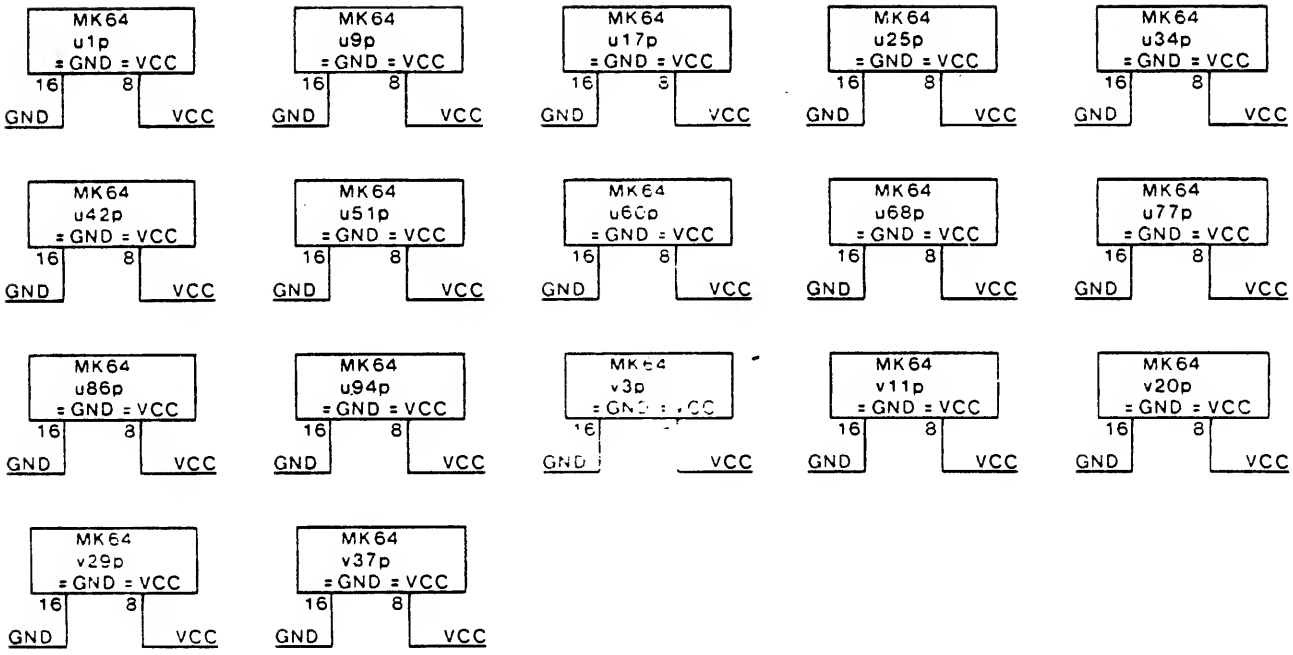
EROX ED	Project MCCP	Address Drivers	File PMCCP07.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 7



Address,RAS,CAS,Write Display Bank

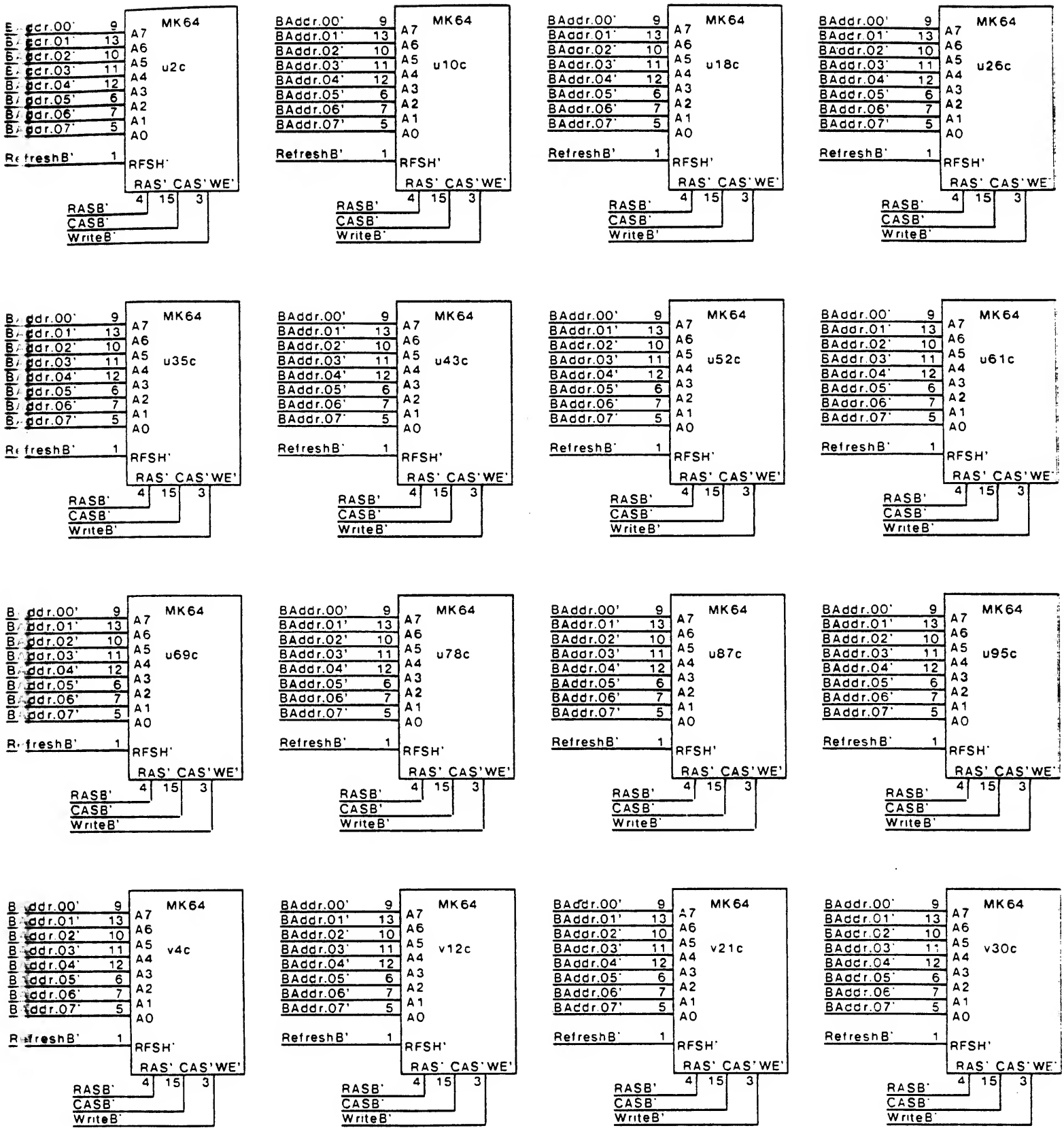
XEROX ED	Project MCCP	Address,RAS,CAS,Write Display Bank	File PMCCP08.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 8





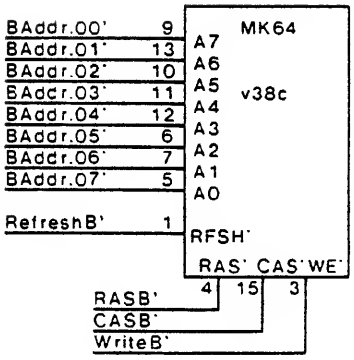
Address,RAS,CAS,Write Display Bank

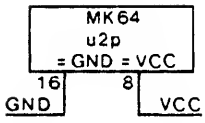
XEROX ED	Project MCCP	Address,RAS,CAS,Write Display Bank	File PMCCP09.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 9

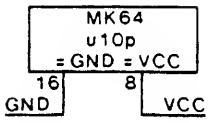


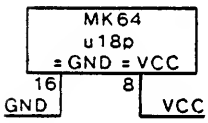
Mem. Control/ Bank B

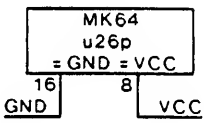
XEROX ED	Project MCCP	Mem. Control/ Bank B	File PMCCP10.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 10

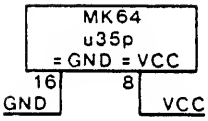

BAddr.00' 9
BAddr.01' 13
BAddr.02' 10
BAddr.03' 11
BAddr.04' 12
BAddr.05' 6
BAddr.06' 7
BAddr.07' 5
RefreshB' 1
MK64
A7
A6
A5
A4
A3
A2
A1
A0
v38c
RFSH'
RAS' CAS' WE'
4 15 3
RASB'
CASB'
WriteB'

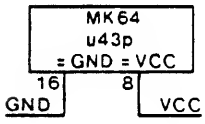

MK64
u2p
= GND = VCC
16 8
GND VCC

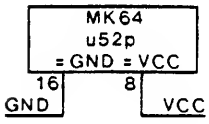

MK64
u10p
= GND = VCC
16 8
GND VCC

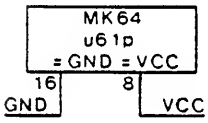

MK64
u18p
= GND = VCC
16 8
GND VCC

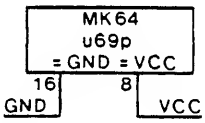

MK64
u26p
= GND = VCC
16 8
GND VCC

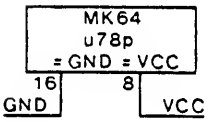

MK64
u35p
= GND = VCC
16 8
GND VCC

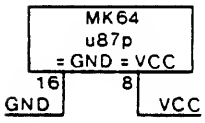

MK64
u43p
= GND = VCC
16 8
GND VCC

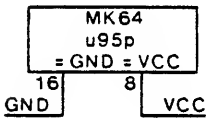

MK64
u52p
= GND = VCC
16 8
GND VCC

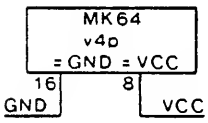

MK64
u61p
= GND = VCC
16 8
GND VCC

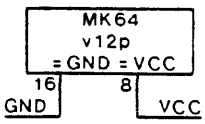

MK64
u69p
= GND = VCC
16 8
GND VCC

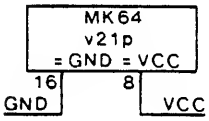

MK64
u78p
= GND = VCC
16 8
GND VCC

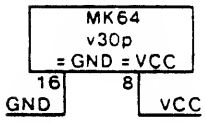

MK64
u87p
= GND = VCC
16 8
GND VCC

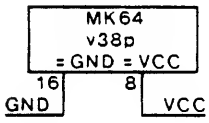

MK64
u95p
= GND = VCC
16 8
GND VCC

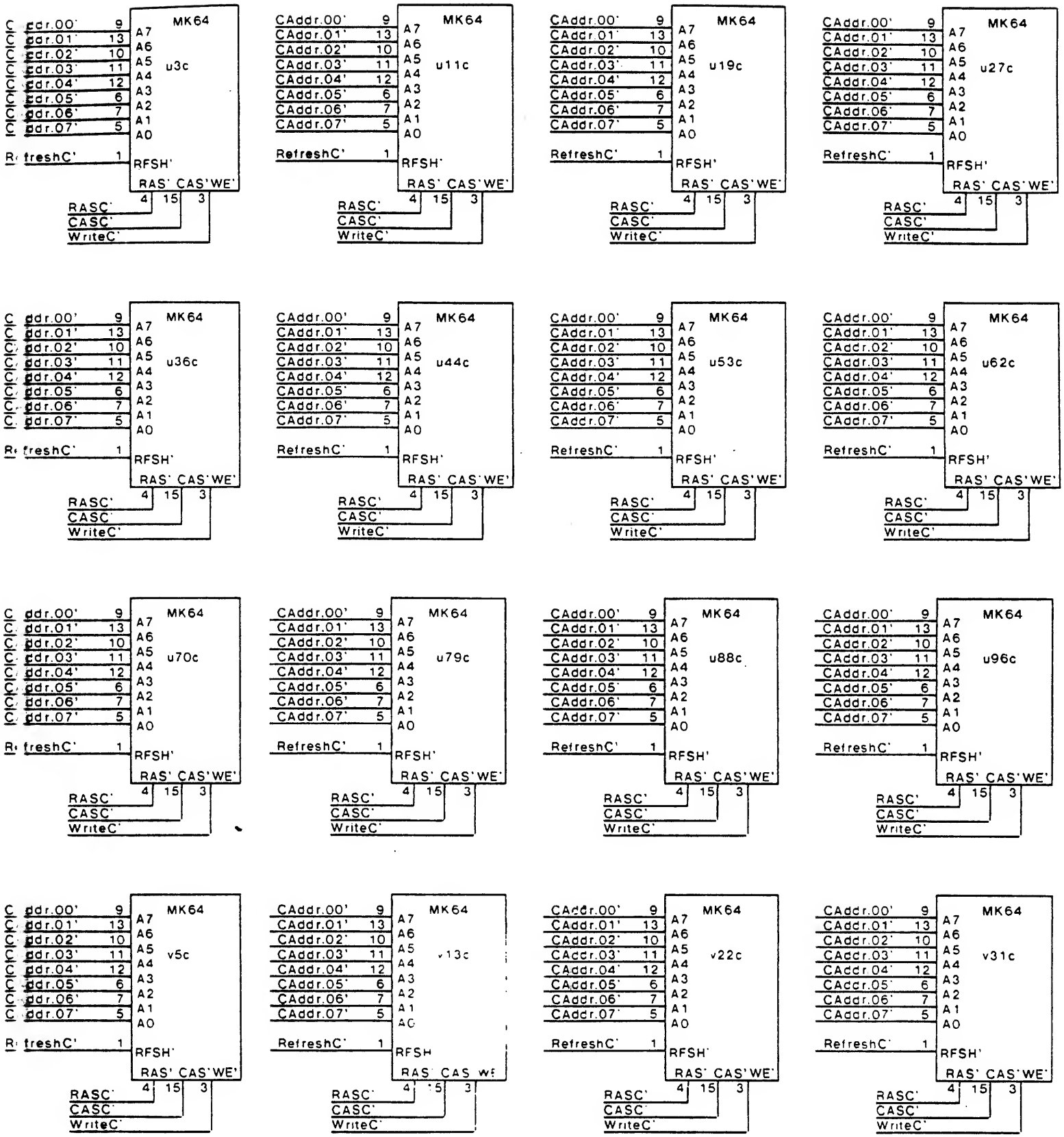

MK64
v4p
= GND = VCC
16 8
GND VCC


MK64
v12p
= GND = VCC
16 8
GND VCC


MK64
v21p
= GND = VCC
16 8
GND VCC

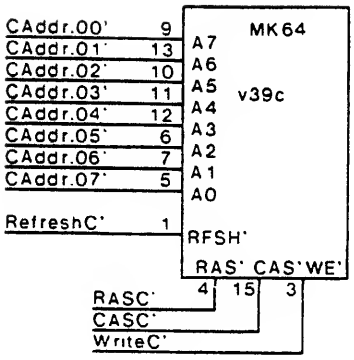

MK64
v30p
= GND = VCC
16 8
GND VCC

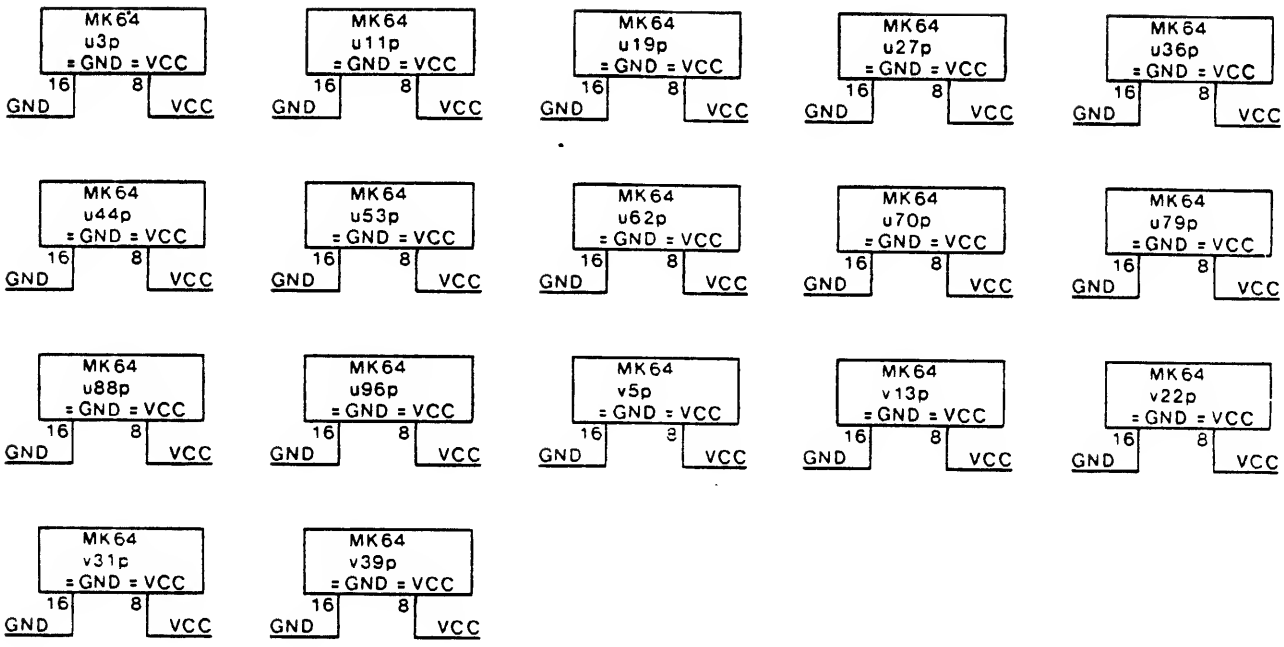

MK64
v38p
= GND = VCC
16 8
GND VCC

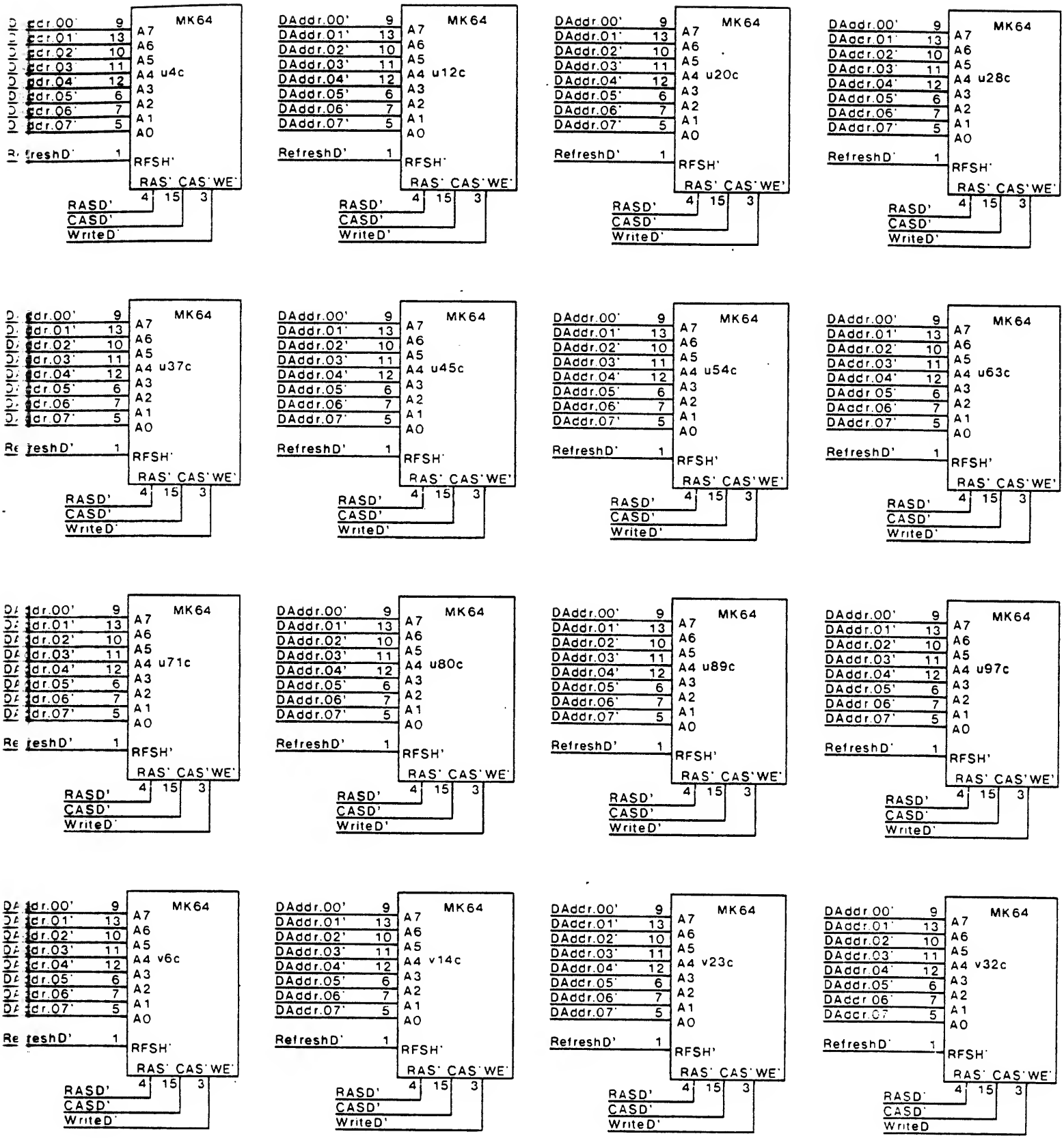


Mem. Control/ Bank C

XEROX ED	Project MCCP	Mem. Control/ Bank C	File PMCCP12.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 12

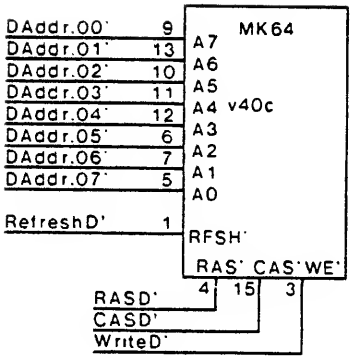

MK64
v39c
CAddr.00' 9
CAddr.01' 13
CAddr.02' 10
CAddr.03' 11
CAddr.04' 12
CAddr.05' 6
CAddr.06' 7
CAddr.07' 5
RefreshC' 1
A7
A6
A5
A4
A3
A2
A1
A0
RFSH'
RAS' CAS' WE'
4 15 3
RASC'
CASC'
WriteC'

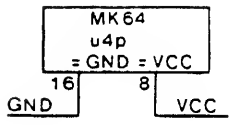

MK64 u3p = GND = VCC
MK64 u11p = GND = VCC
MK64 u19p = GND = VCC
MK64 u27p = GND = VCC
MK64 u36p = GND = VCC
MK64 u44p = GND = VCC
MK64 u53p = GND = VCC
MK64 u62p = GND = VCC
MK64 u70p = GND = VCC
MK64 u79p = GND = VCC
MK64 u88p = GND = VCC
MK64 u96p = GND = VCC
MK64 v5p = GND = VCC
MK64 v13p = GND = VCC
MK64 v22p = GND = VCC
MK64 v31p = GND = VCC
MK64 v39p = GND = VCC
16
8
GND
VCC

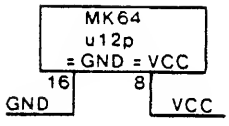


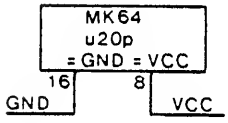
Mem. Control/ Bank D

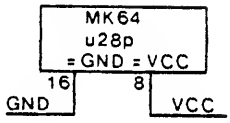
XEROX ED	Project MCCP	Mem. Control/ Bank D	File PMCCP14.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 14

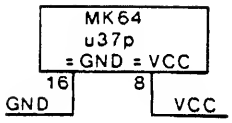

DAddr.00' 9
DAddr.01' 13
DAddr.02' 10
DAddr.03' 11
DAddr.04' 12
DAddr.05' 6
DAddr.06' 7
DAddr.07' 5
RefreshD' 1
MK64
A7
A6
A5
A4
v40c
A3
A2
A1
A0
RFSH'
RAS' CAS' WE'
4 15 3
RASD'
CASD'
WriteD'

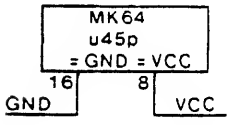

MK64
u4p
= GND = VCC
16
8
GND
VCC

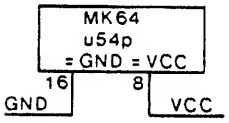

MK64
u12p
= GND = VCC
16
8
GND
VCC

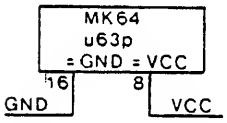

MK64
u20p
= GND = VCC
16
8
GND
VCC

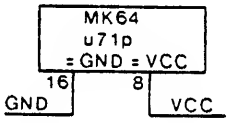

MK64
u28p
= GND = VCC
16
8
GND
VCC

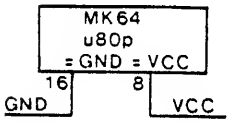

MK64
u37p
= GND = VCC
16
8
GND
VCC

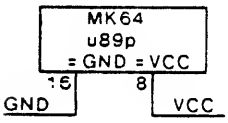

MK64
u45p
= GND = VCC
16
8
GND
VCC

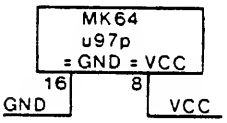

MK64
u54p
= GND = VCC
16
8
GND
VCC

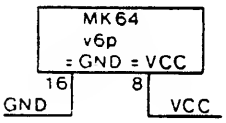

MK64
u63p
= GND = VCC
16
8
GND
VCC

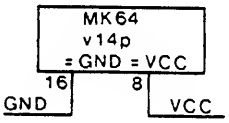

MK64
u71p
= GND = VCC
16
8
GND
VCC

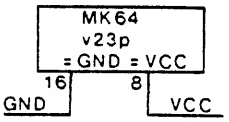

MK64
u80p
= GND = VCC
16
8
GND
VCC

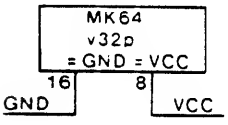

MK64
u89p
= GND = VCC
16
8
GND
VCC

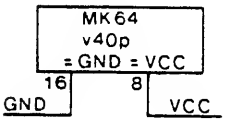

MK64
u97p
= GND = VCC
16
8
GND
VCC

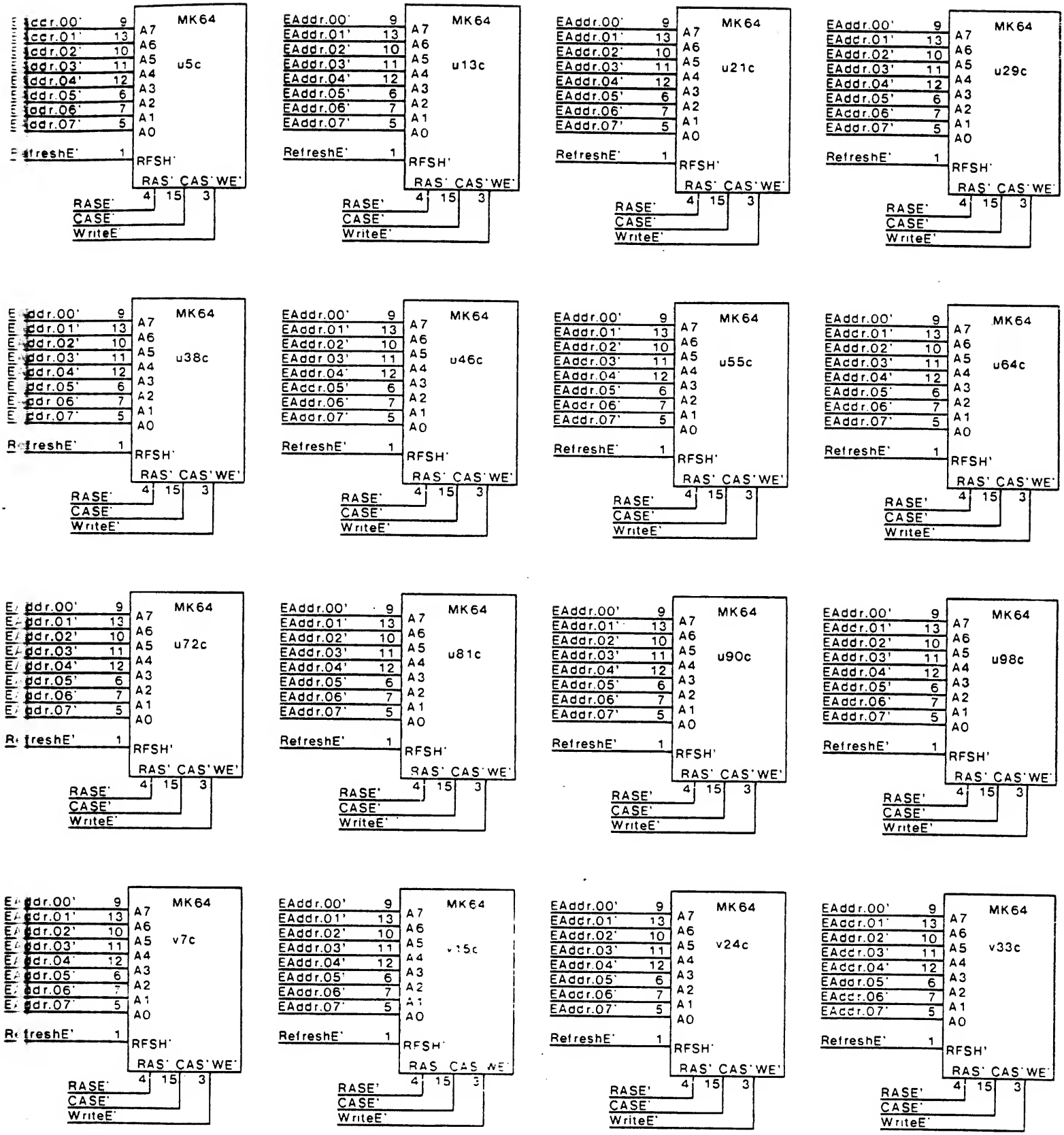

MK64
v6p
= GND = VCC
16
8
GND
VCC


MK64
v14p
= GND = VCC
16
8
GND
VCC


MK64
v23p
= GND = VCC
16
8
GND
VCC

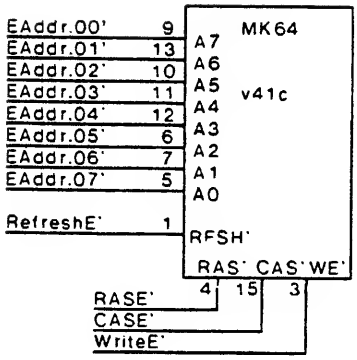

MK64
v32p
= GND = VCC
16
8
GND
VCC

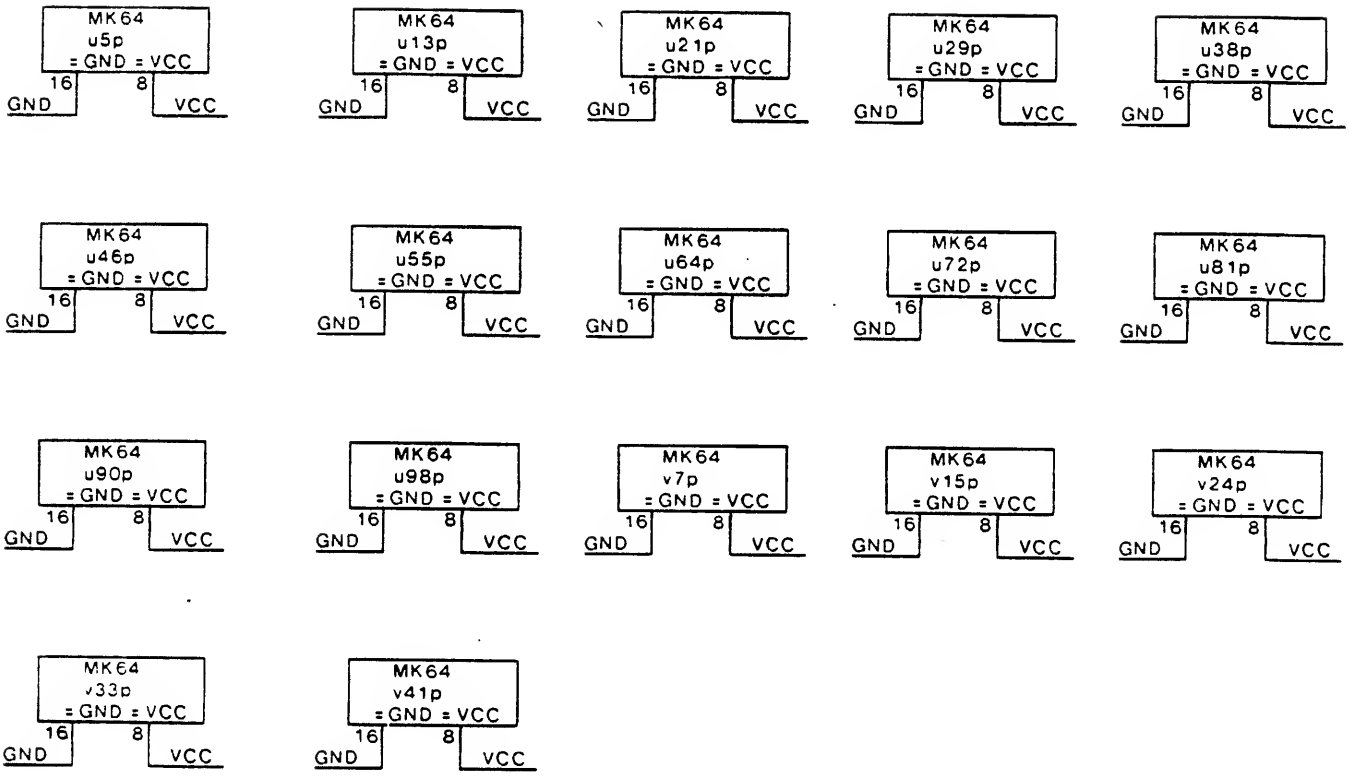

MK64
v40p
= GND = VCC
16
8
GND
VCC

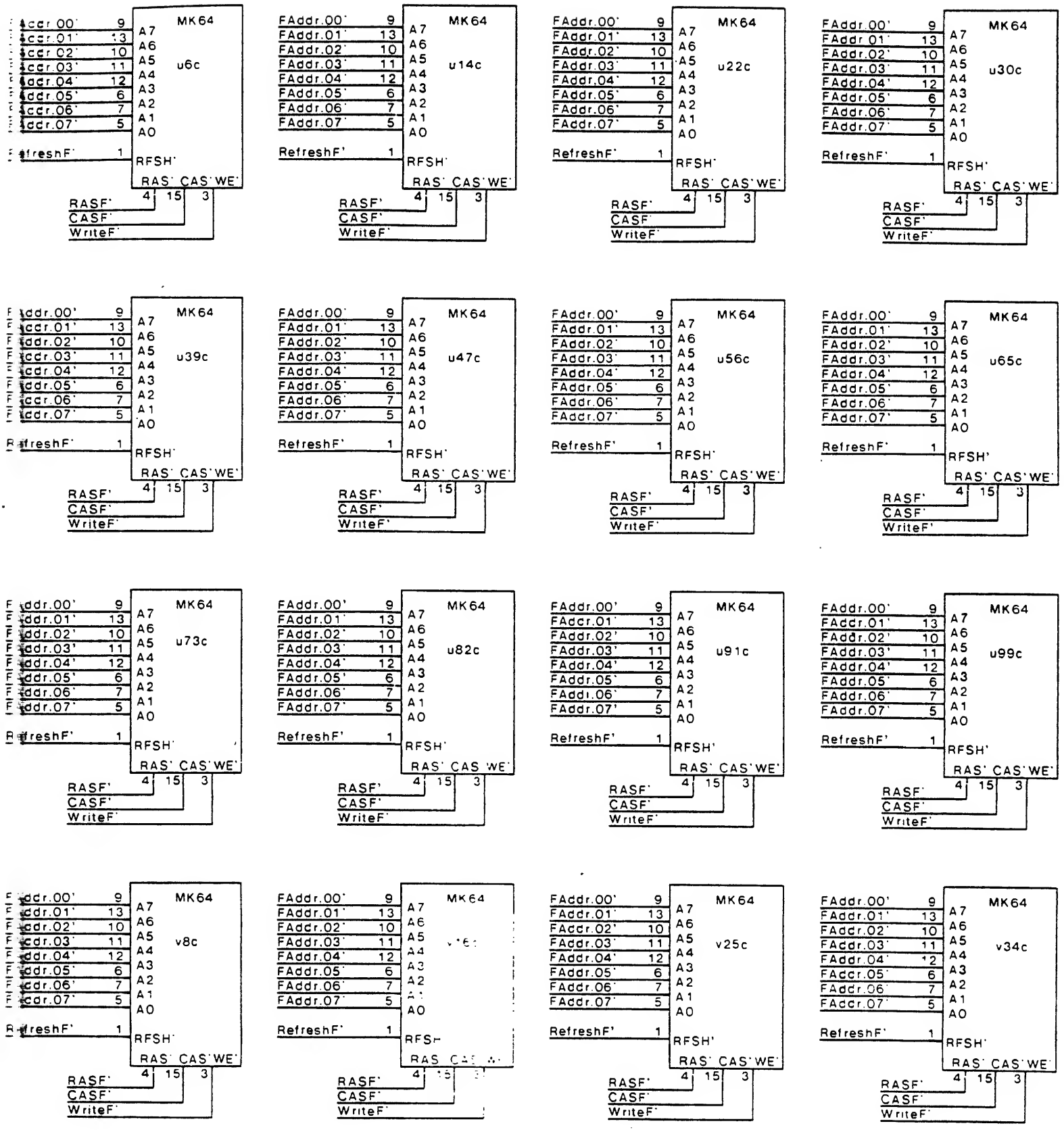


Mem. Control/ Bank E

XEROX ED	Project MCCP	Mem. Control/ Bank E	File PMCCP16.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 16

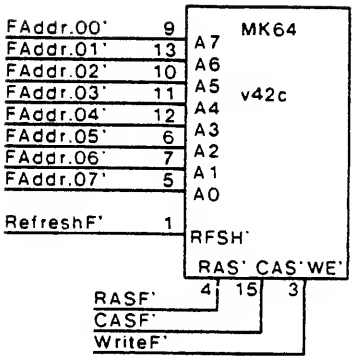

EAddr.00' 9
EAddr.01' 13
EAddr.02' 10
EAddr.03' 11
EAddr.04' 12
EAddr.05' 6
EAddr.06' 7
EAddr.07' 5
RefreshE' 1
MK64
A7
A6
A5
A4
A3
A2
A1
A0
v41c
RFSH'
RAS' CAS' WE'
4 15 3
RASE'
CASE'
WriteE'

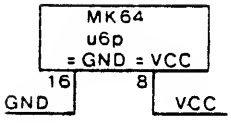

MK64 u5p = GND = VCC
MK64 u13p = GND = VCC
MK64 u21p = GND = VCC
MK64 u29p = GND = VCC
MK64 u38p = GND = VCC
MK64 u46p = GND = VCC
MK64 u55p = GND = VCC
MK64 u64p = GND = VCC
MK64 u72p = GND = VCC
MK64 u81p = GND = VCC
MK64 u90p = GND = VCC
MK64 u98p = GND = VCC
MK64 v7p = GND = VCC
MK64 v15p = GND = VCC
MK64 v24p = GND = VCC
MK64 v33p = GND = VCC
MK64 v41p = GND = VCC
16
8
GND
VCC

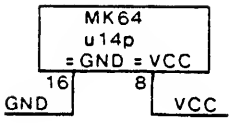


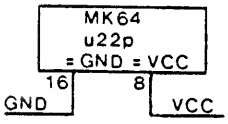
Mem. Control/ Bank F (no dram required for 256k dram module)

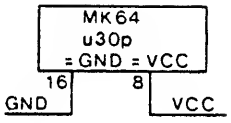
XEROX ED	Project MCCP	Mem. Control/ Bank F	File PMCCP18.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 18

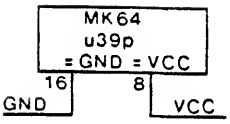


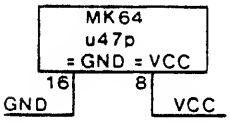


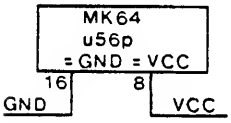


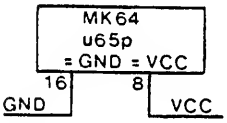


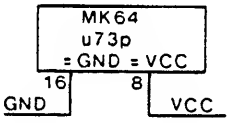


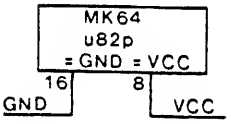


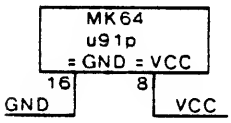


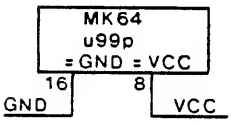


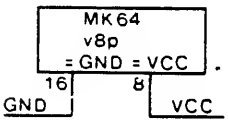


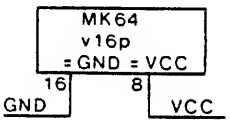


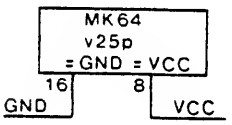


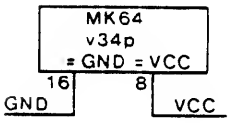


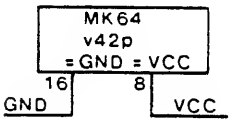






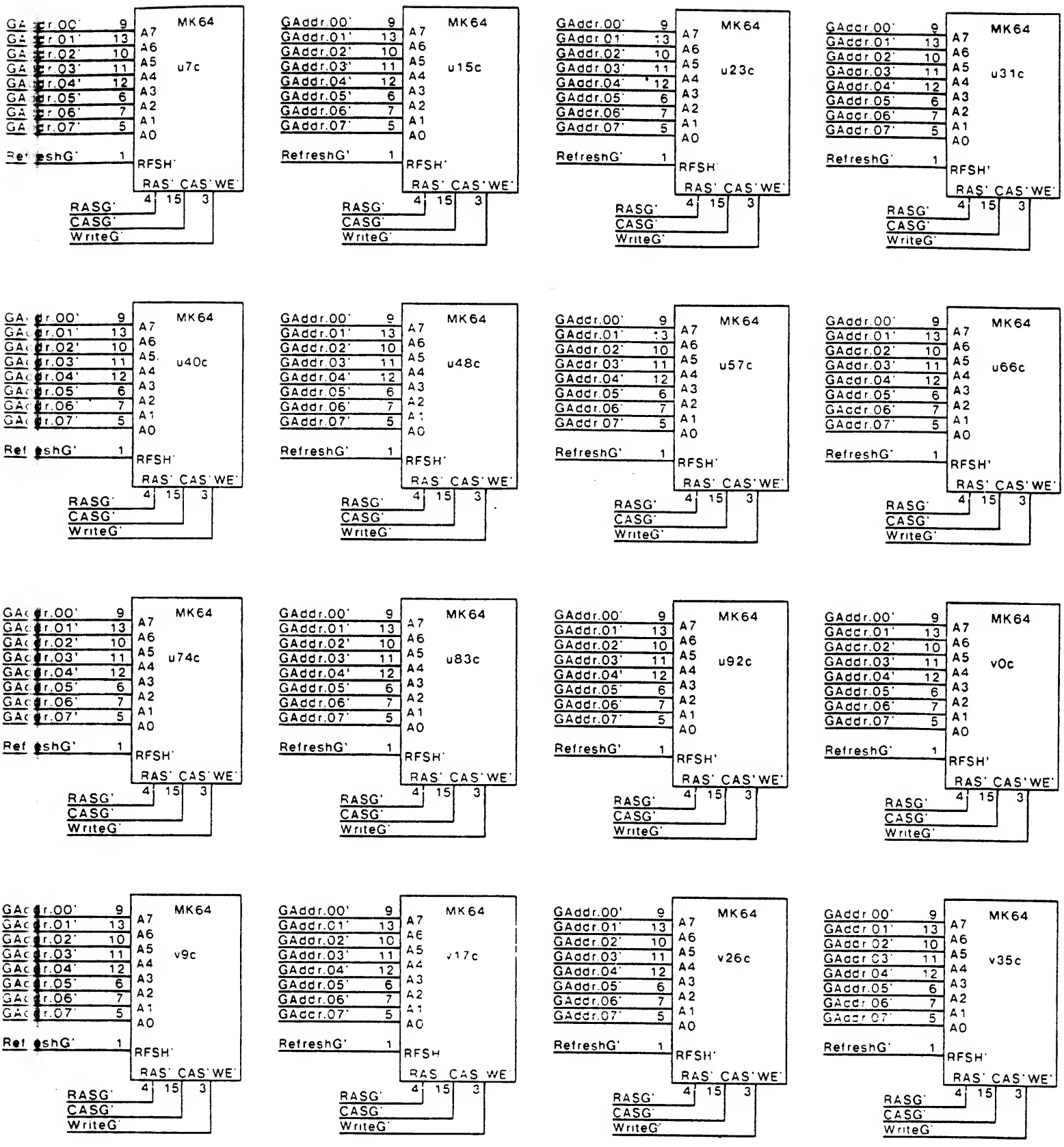






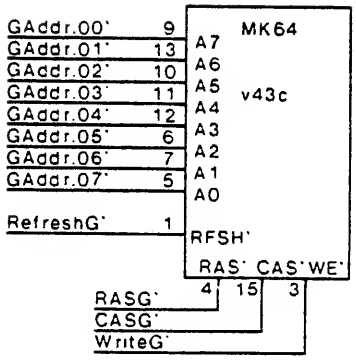
Mem. Control/ Bank F (no dram required for 256k dram module)

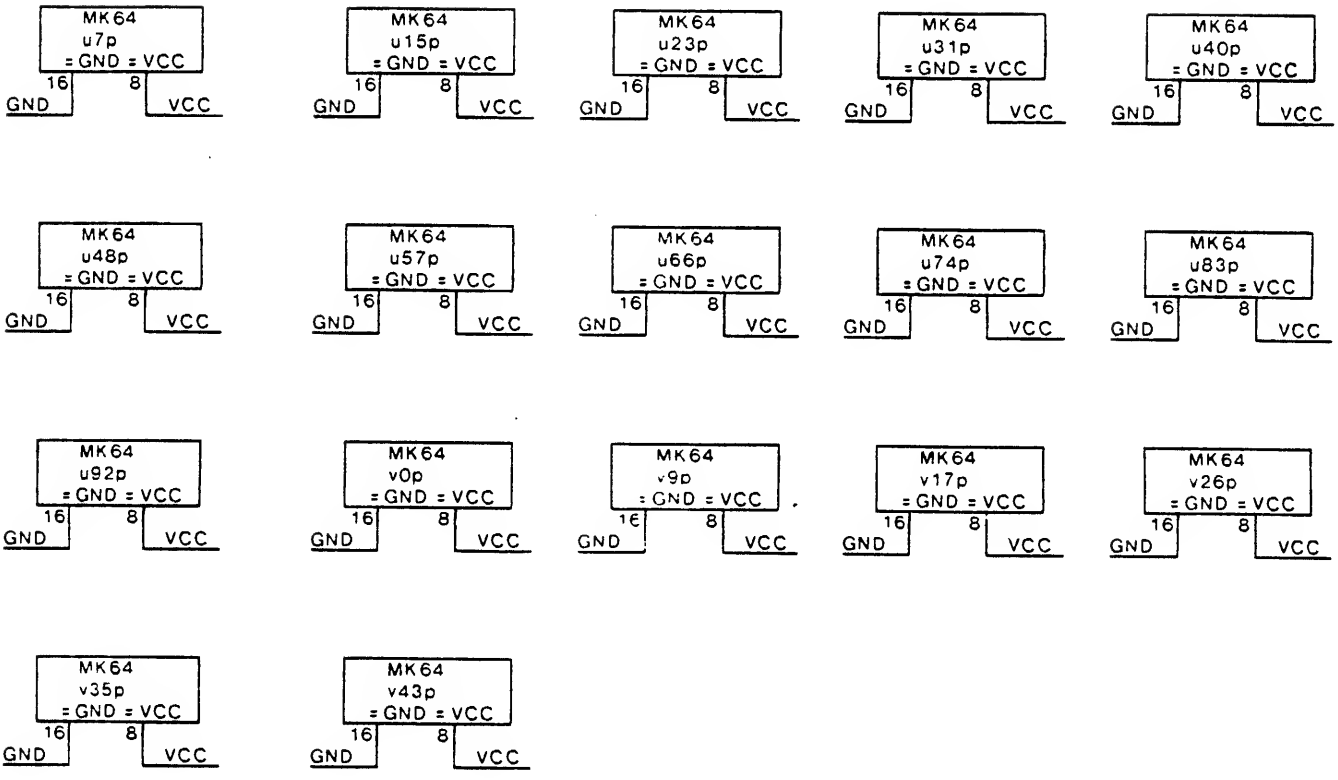
XEROX ED	Project		File	Designer	Rev	Date	Page
	MCCP	Mem. Control/ Bank F	PMCCP19.sil	S. Ando	A	8/31/83	19



Mem. Control/ Bank G (no dram required for 256k dram module)

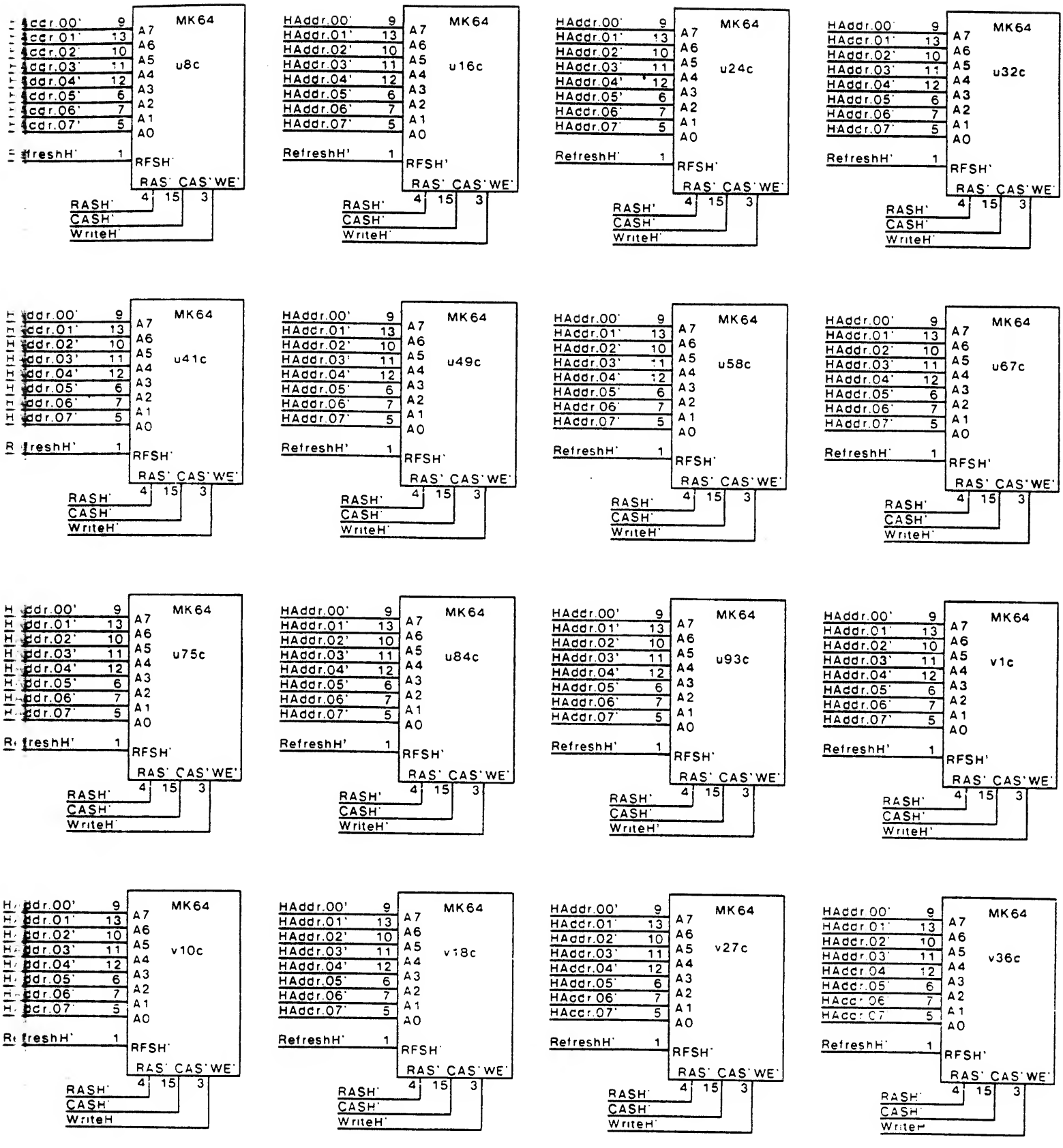
XEROX ED	Project		File	Designer	Rev	Date	Page
	MCCP	Mem. Control/ Bank G	PMCCP20.sil	S. Ando	A	8/31/83	20





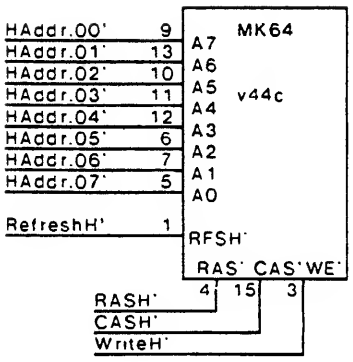
Mem. Control/ Bank G (no dram required for 256k dram module)

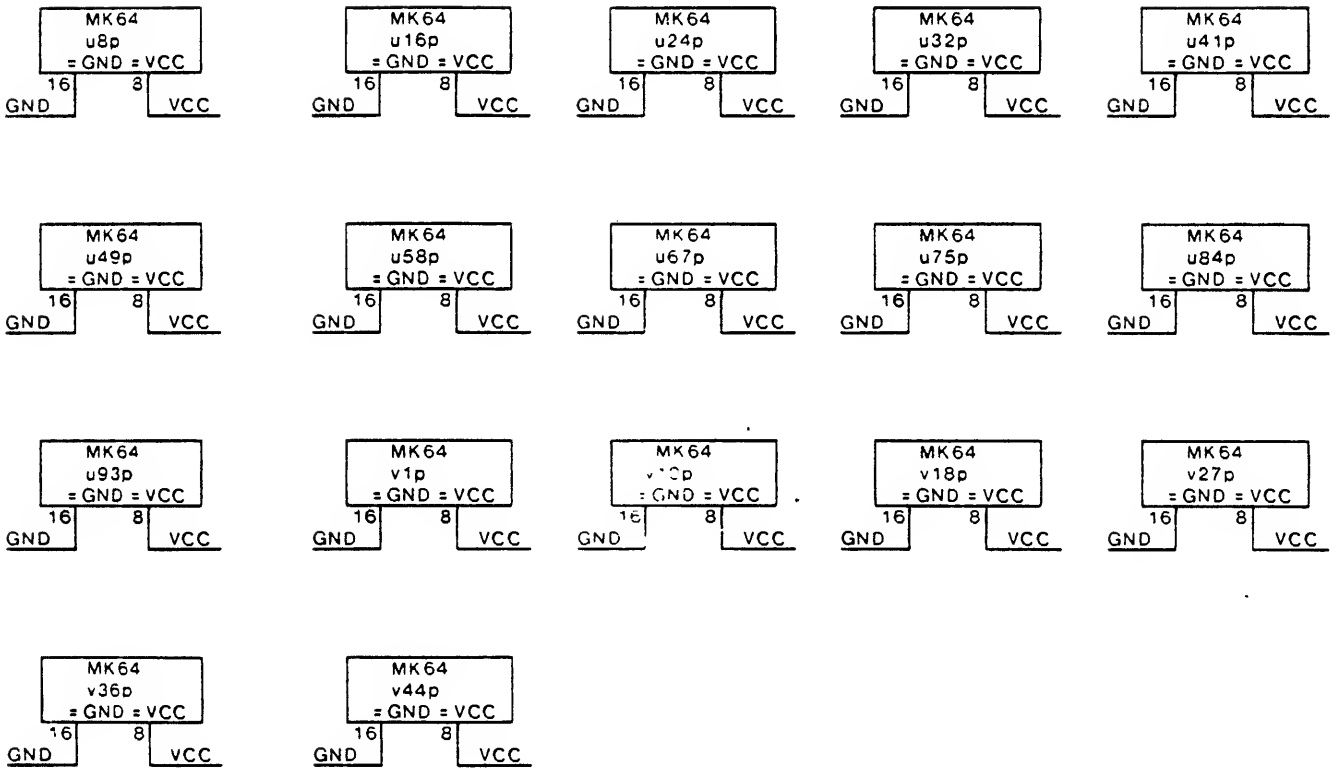
XEROX ED	Project MCCP	Mem. Control/ Bank G	File PMCCP21.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 21



Mem. Control/ Bank H (no dram required for 256k dram module)

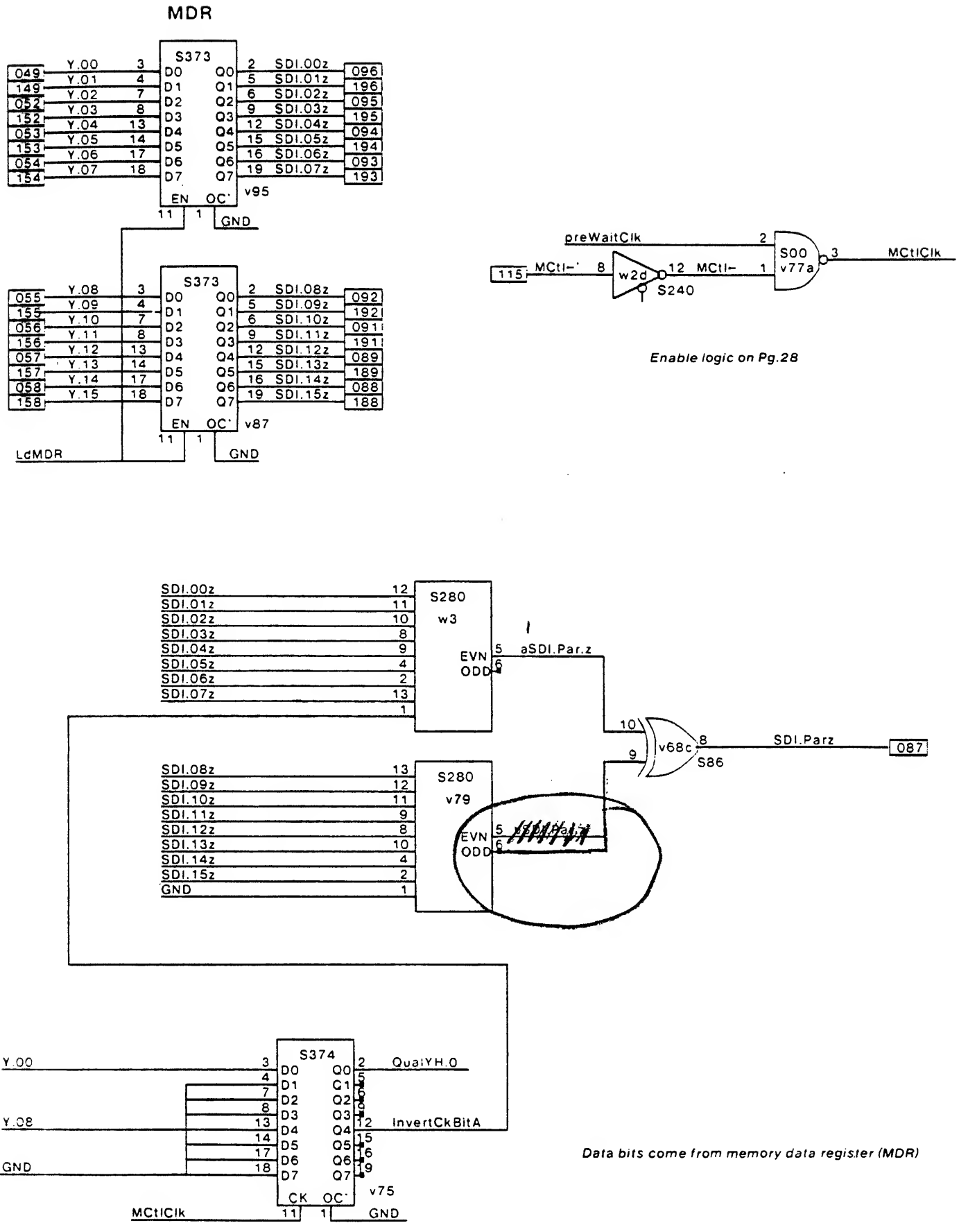
XEROX ED	Project MCCP	Mem. Control/ Bank H	File PMCCP22.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 22





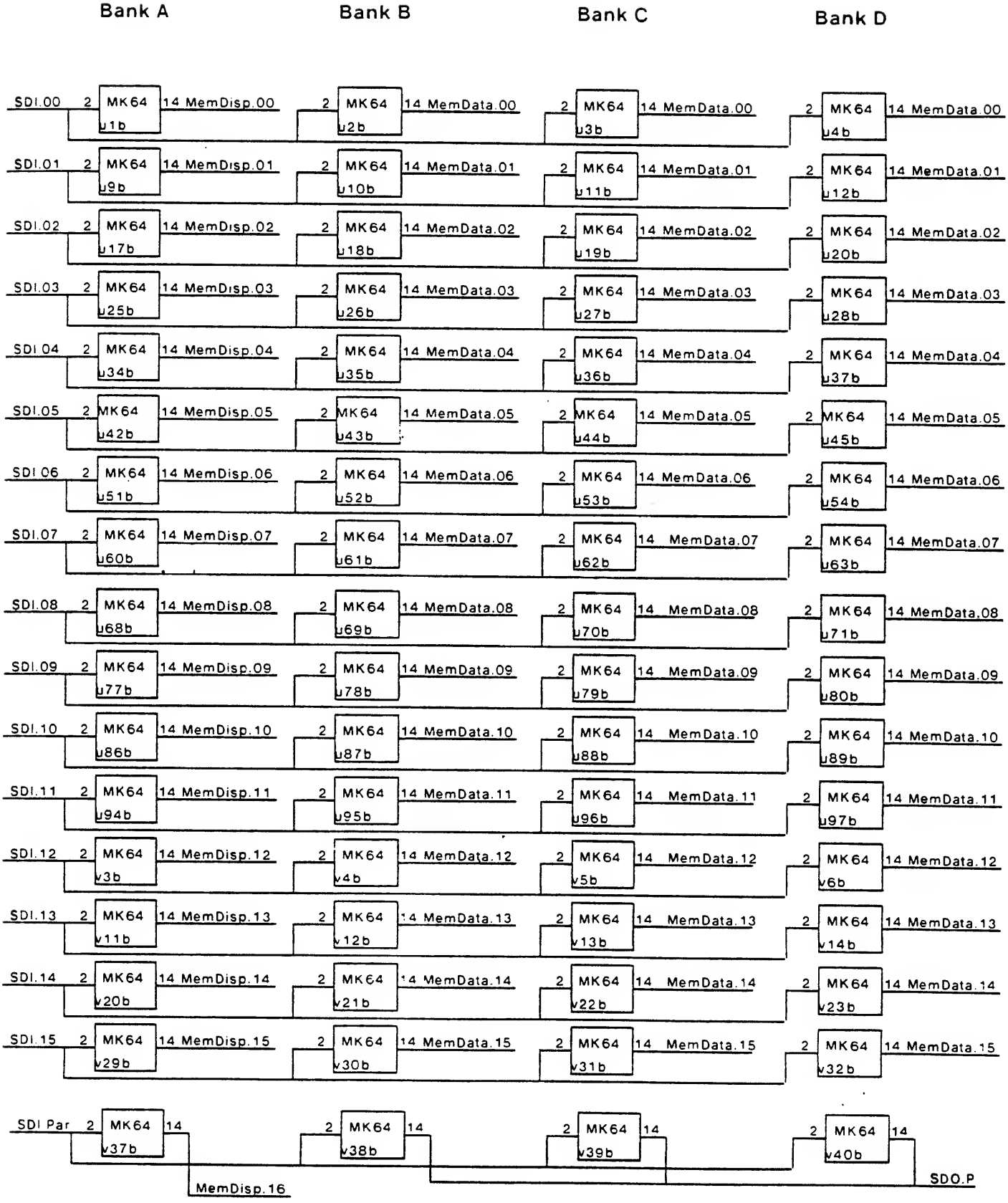
Mem. Controi/ Bank H (no dram required for 256k dram module)

XEROX ED	Project		File	Designer	Rev	Date	Page
	MCCP	Mem. Control/ Bank H	PMCCP23.sil	S. Ando	A	8/31/83	23



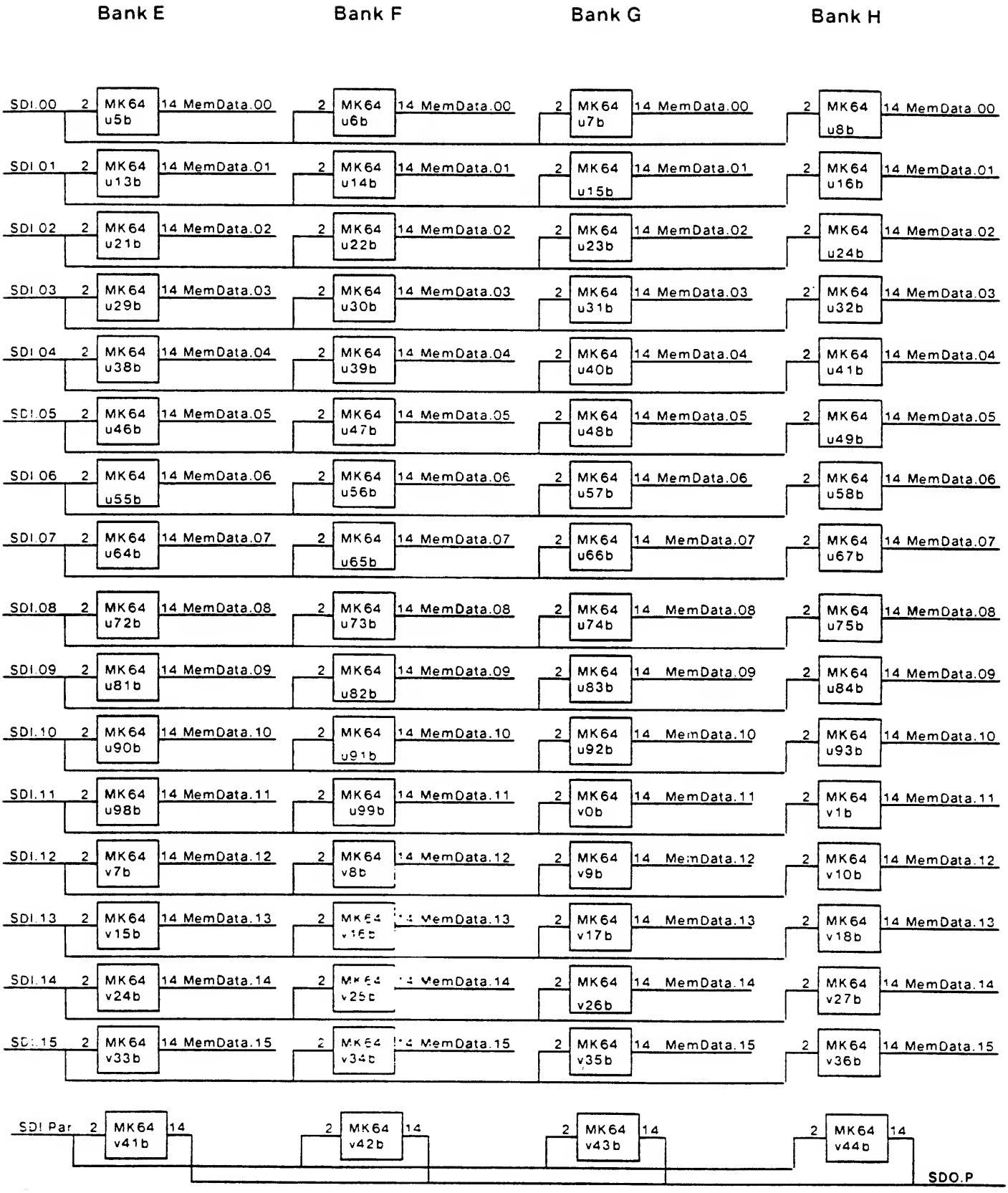
Mem. Data Reg., Mem. Ctl. Reg. & Parity Bit Generator

XEROX ED	Project MCCP	Mem. Data Reg., Mem. Ctl. Reg. & Parity Bit Generator	File PMCCP24.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 24



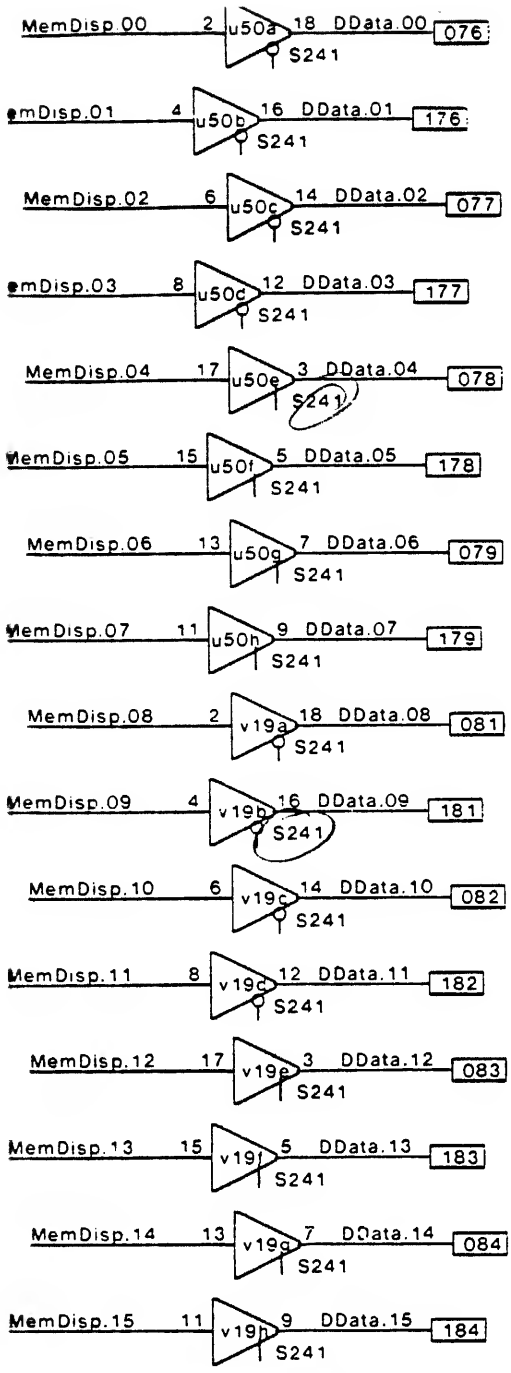
Work Station Memory

XEROX ED	Project MCCP	Work Station Memory	File PMCCP25.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 25

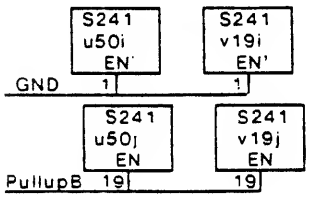


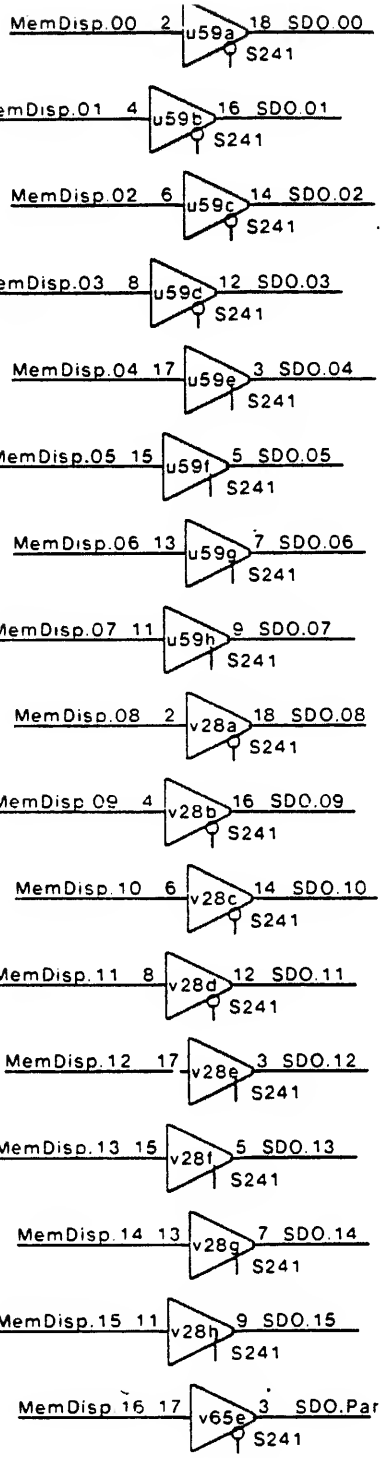
Work Station Memory

XEROX ED	Project MCCP	Work Station Memory	File PMCCP26.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 26

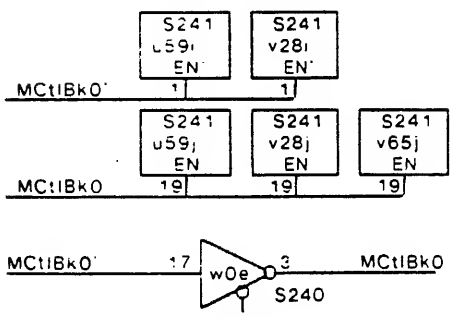


Display Data Buffers

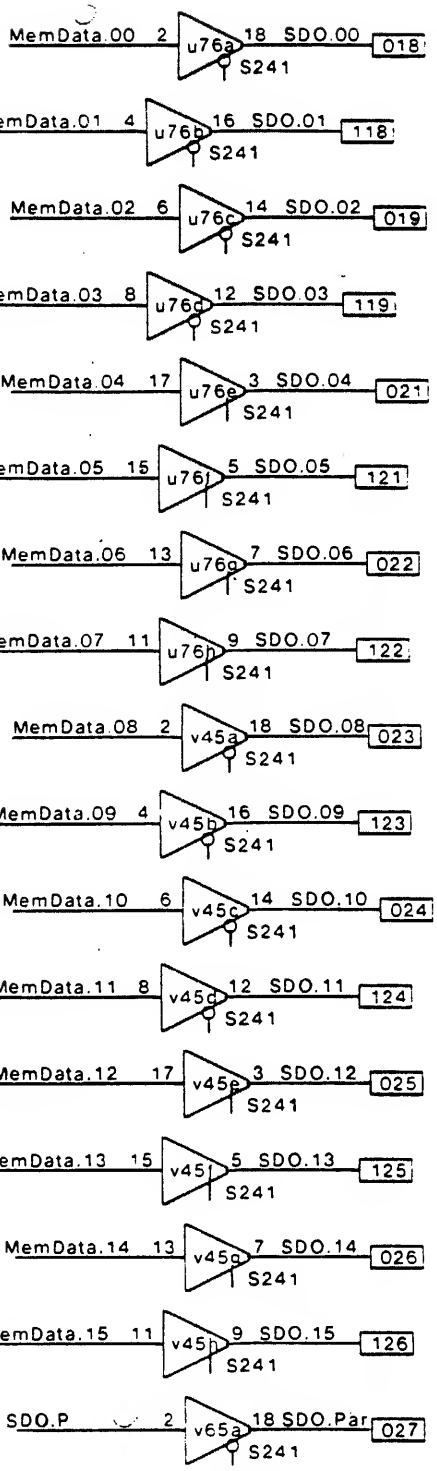




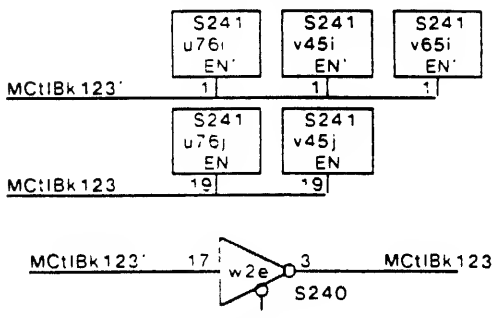
Main Data Buffers



Enable logic on Pg. 28



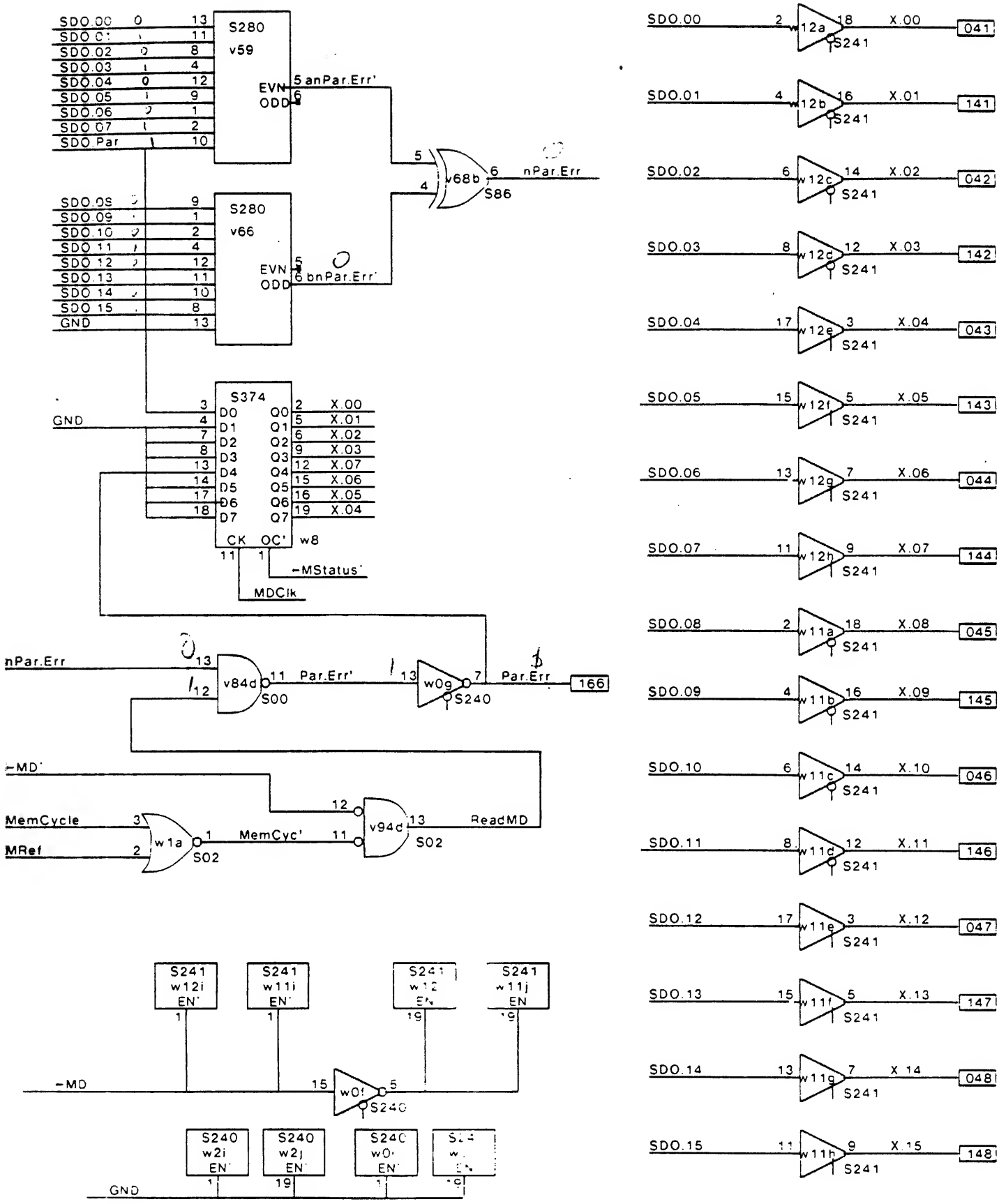
Main Data Buffers



Enable logic on Pg. 28

Data Buffers

XEROX ED	Project MCCP	Data Buffers	File PMCCP27.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 27

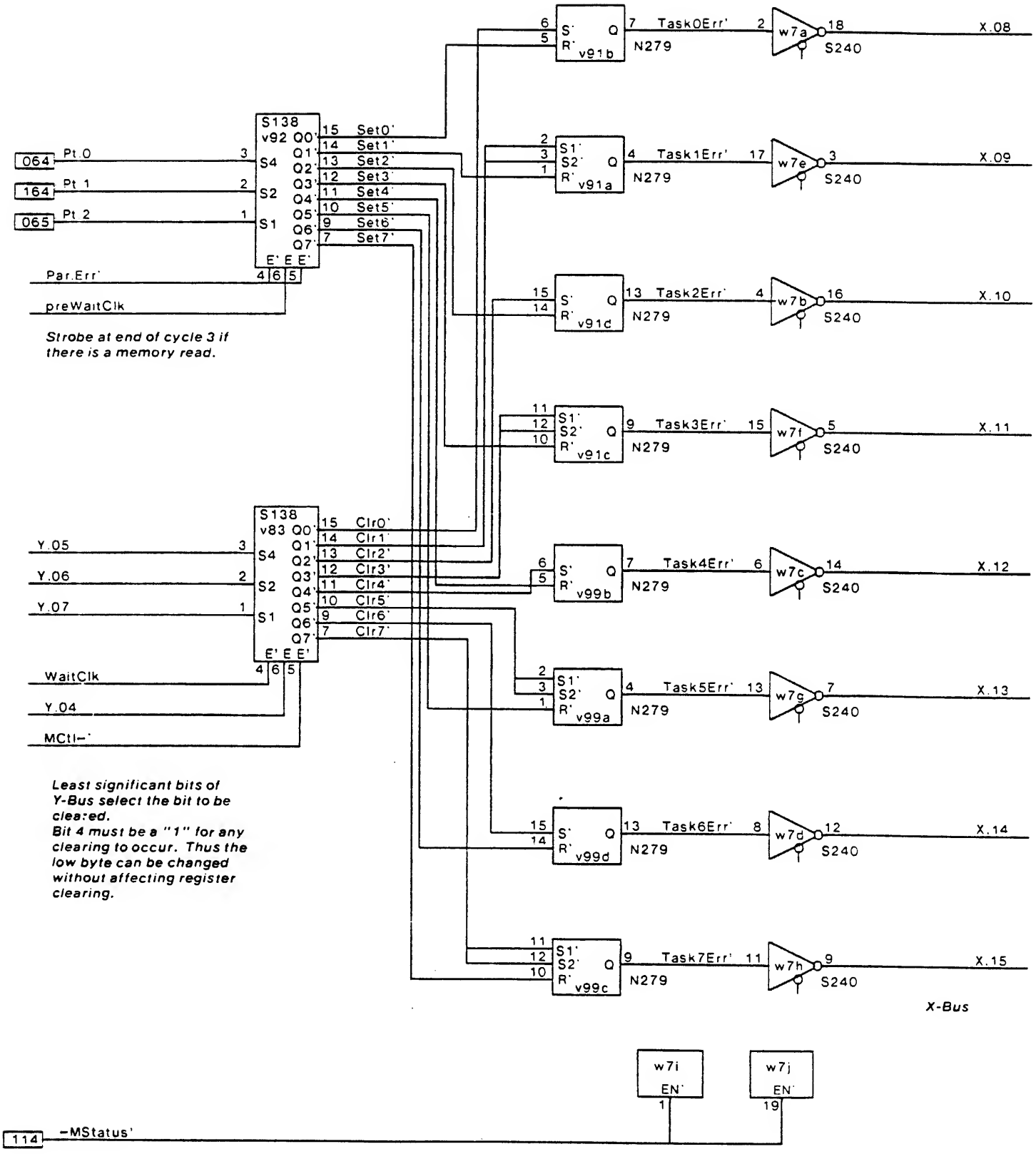


Parity Error & Data Paths

XEROX ED	Project MCCP	Parity.Error & Data Paths	File PMCCP28.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 28

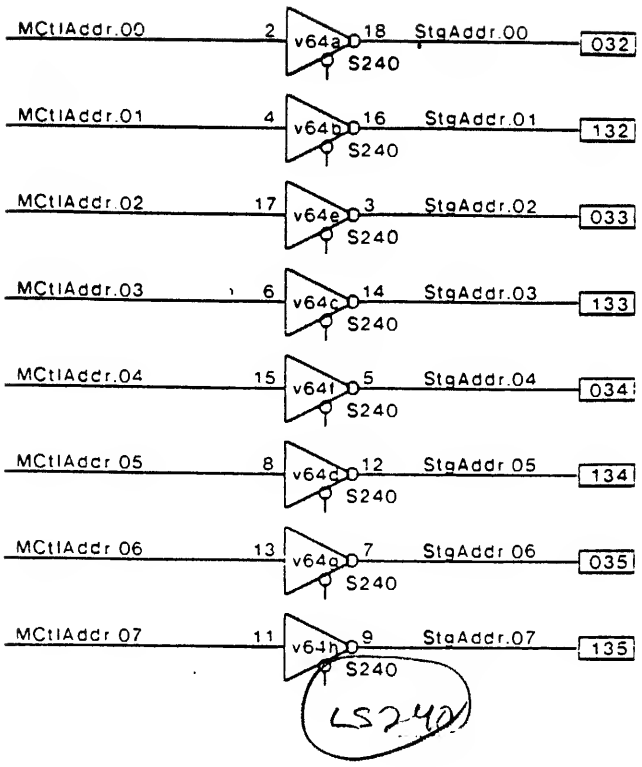
Errors Register

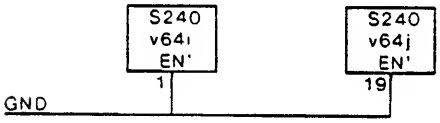
Bit is 1 if there was an error.



Error Log Register

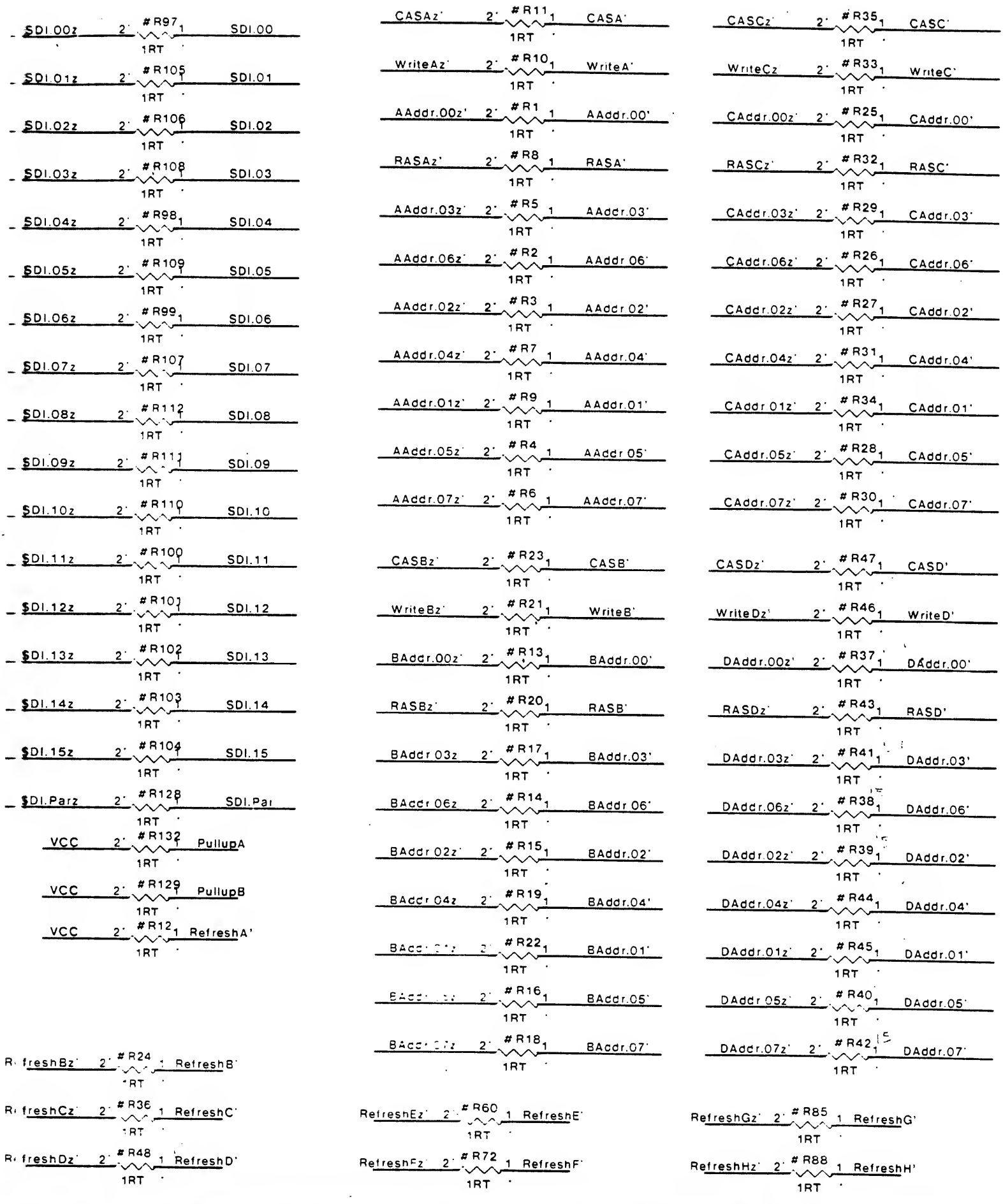
XEROX ED	Project		File	Designer	Rev	Date	Page
	MCCP	Error Log Register	PMCCP29.sil	S. Ando	A	8/31/83	29





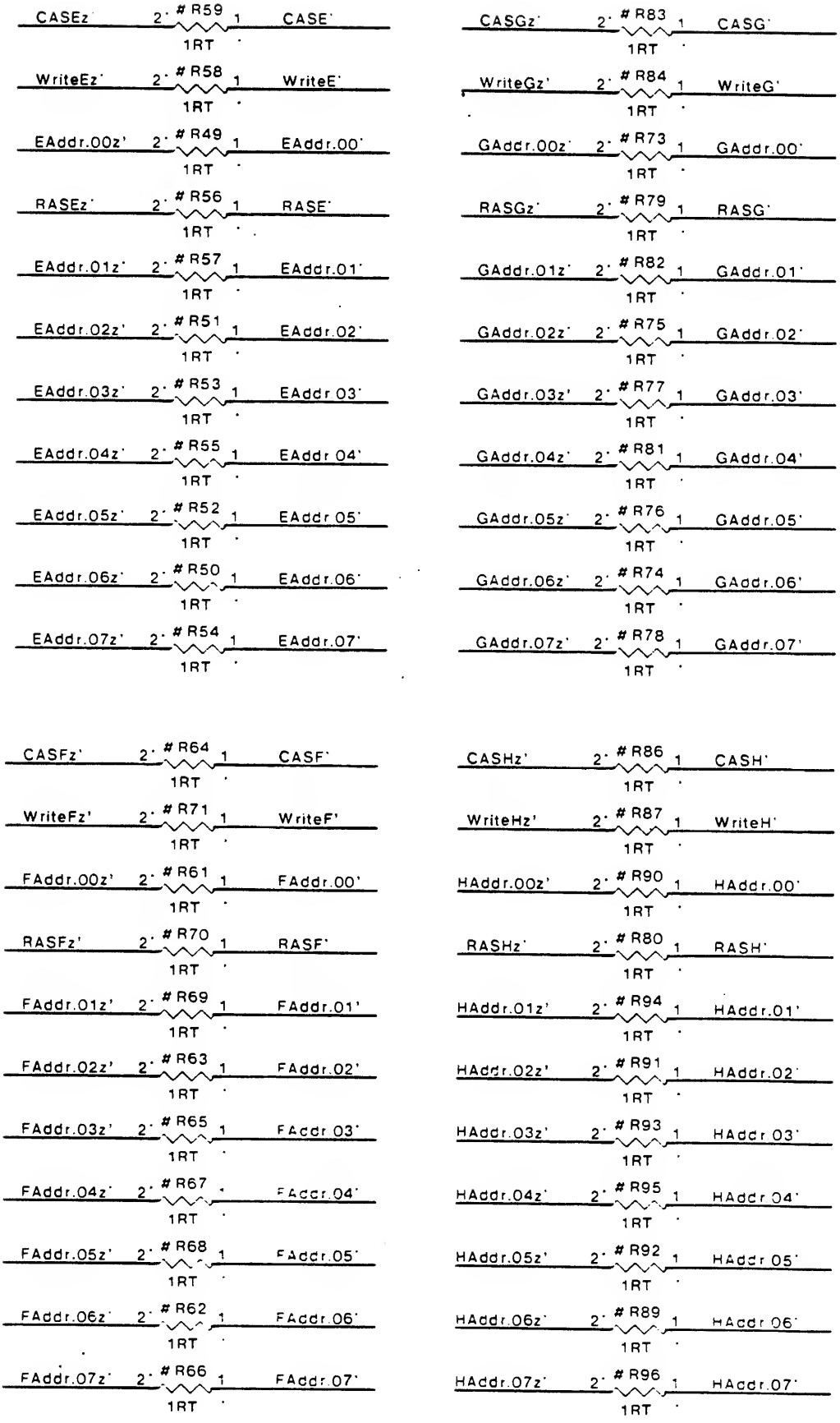
MSC Address Selection

XEROX ED	Project MCCP	MSC Address Selection	File PMCCP30.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 30



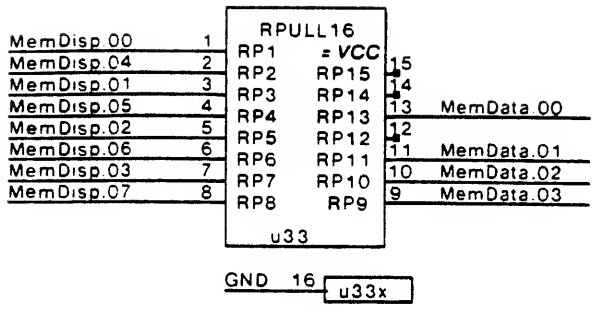
Discrete Resistors

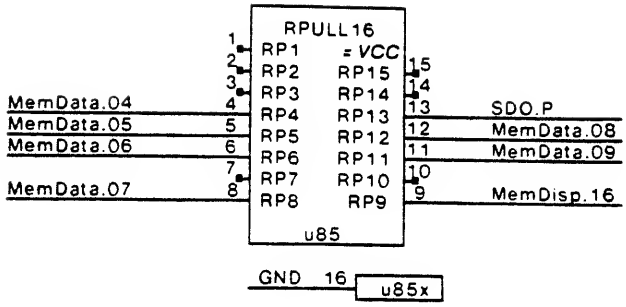
XEROX ED	Project MCCP	Discrete Resistors	File PMCCP31.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 31

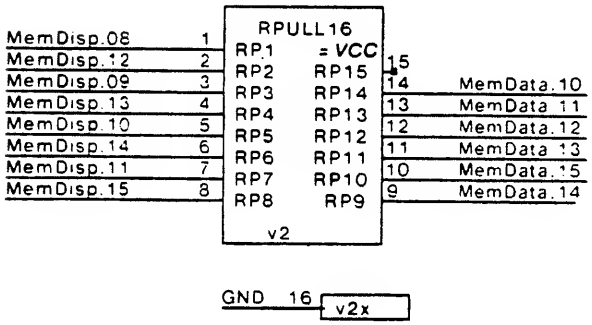


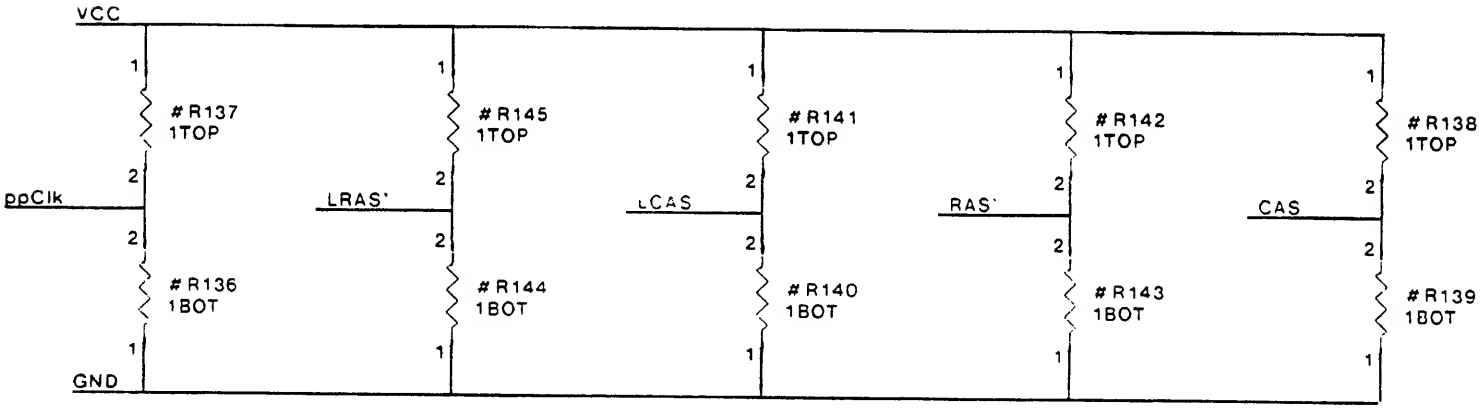
Discrete Resistors

XEROX ED	Project MCCP	Discrete Resistors	File PMCCP32.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 32



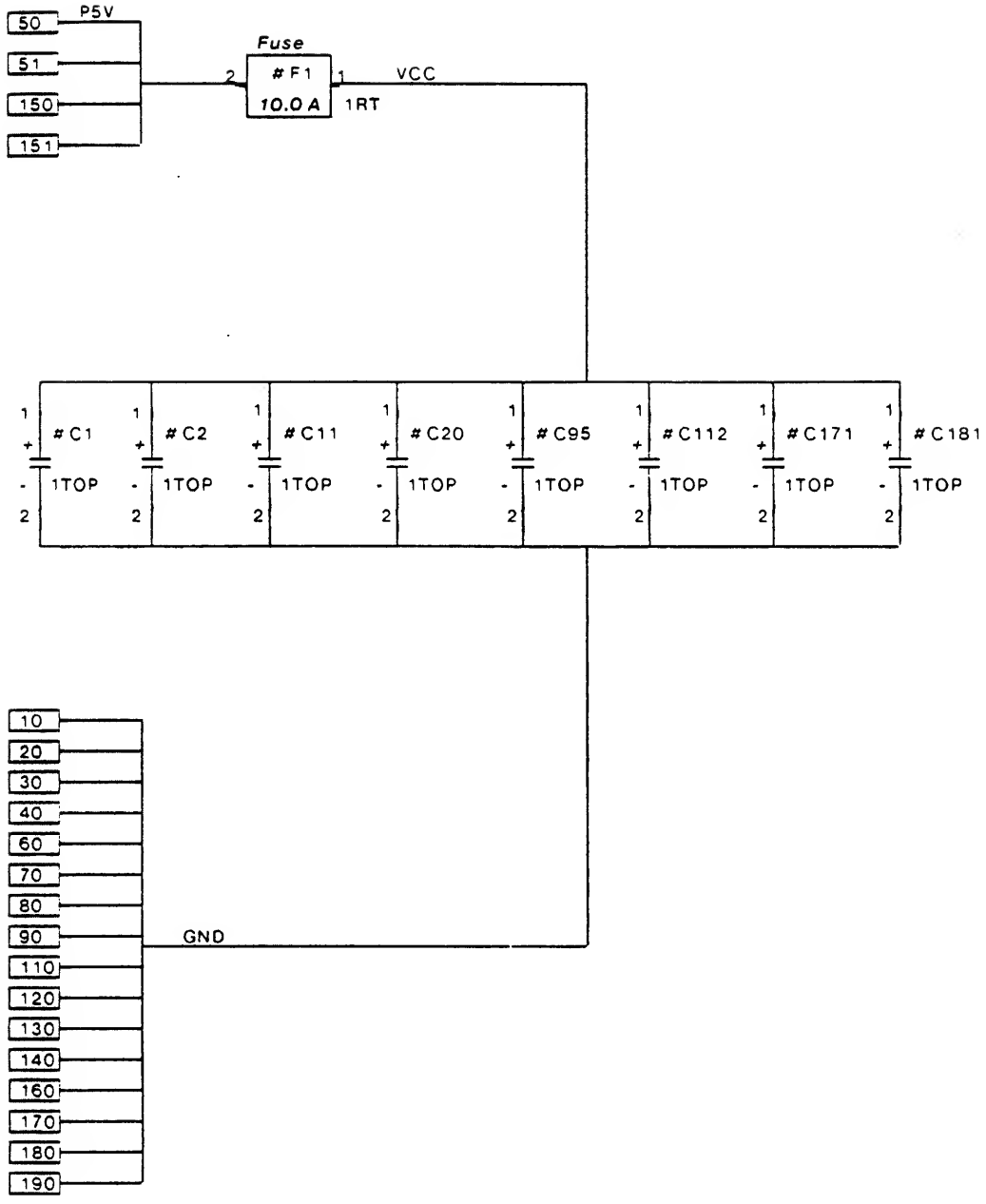






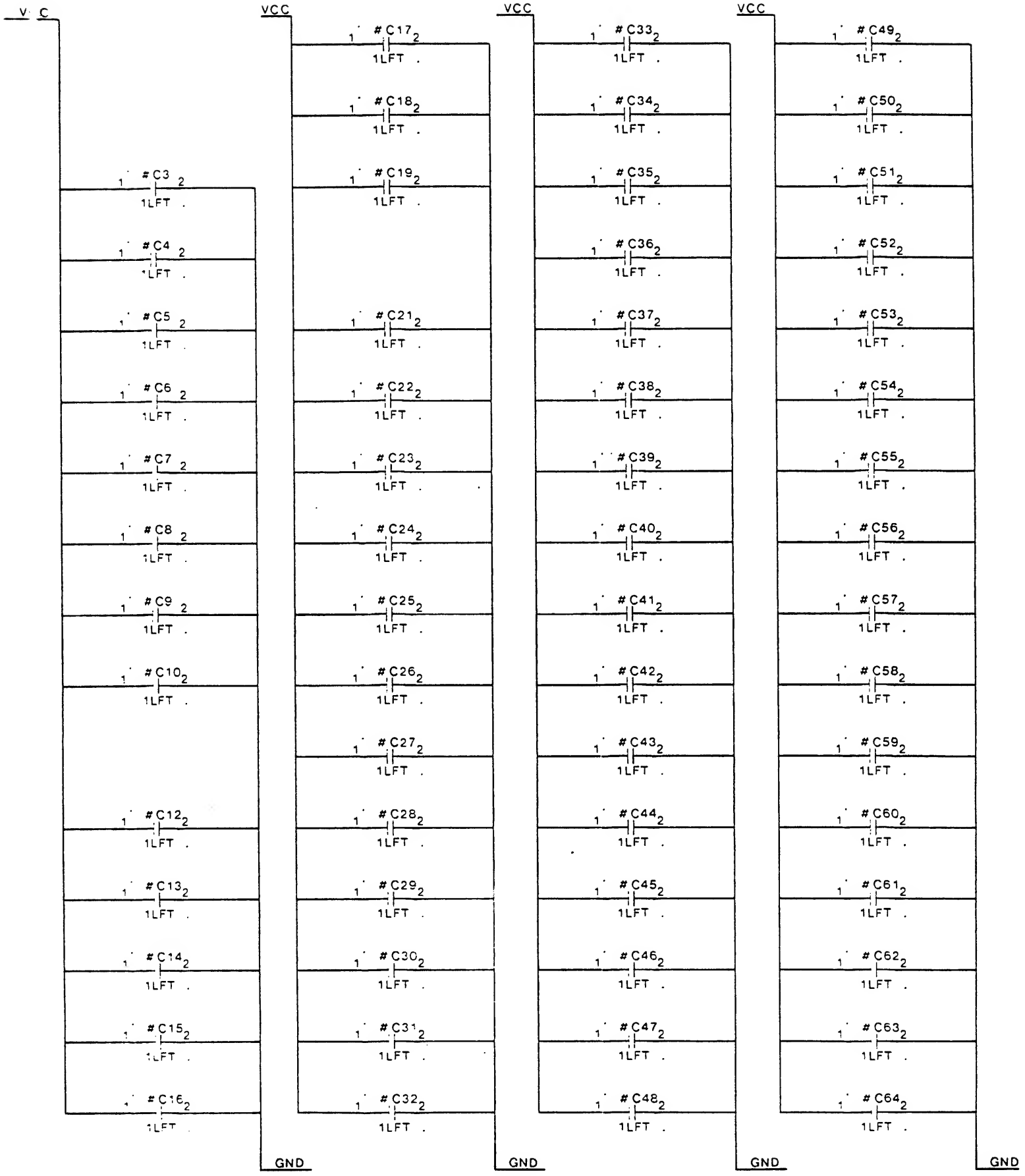
Resistor DIPs, Termination

XEROX ED	Project MCCP	Resistor DIPs. Termination	File PMCCP33.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 33



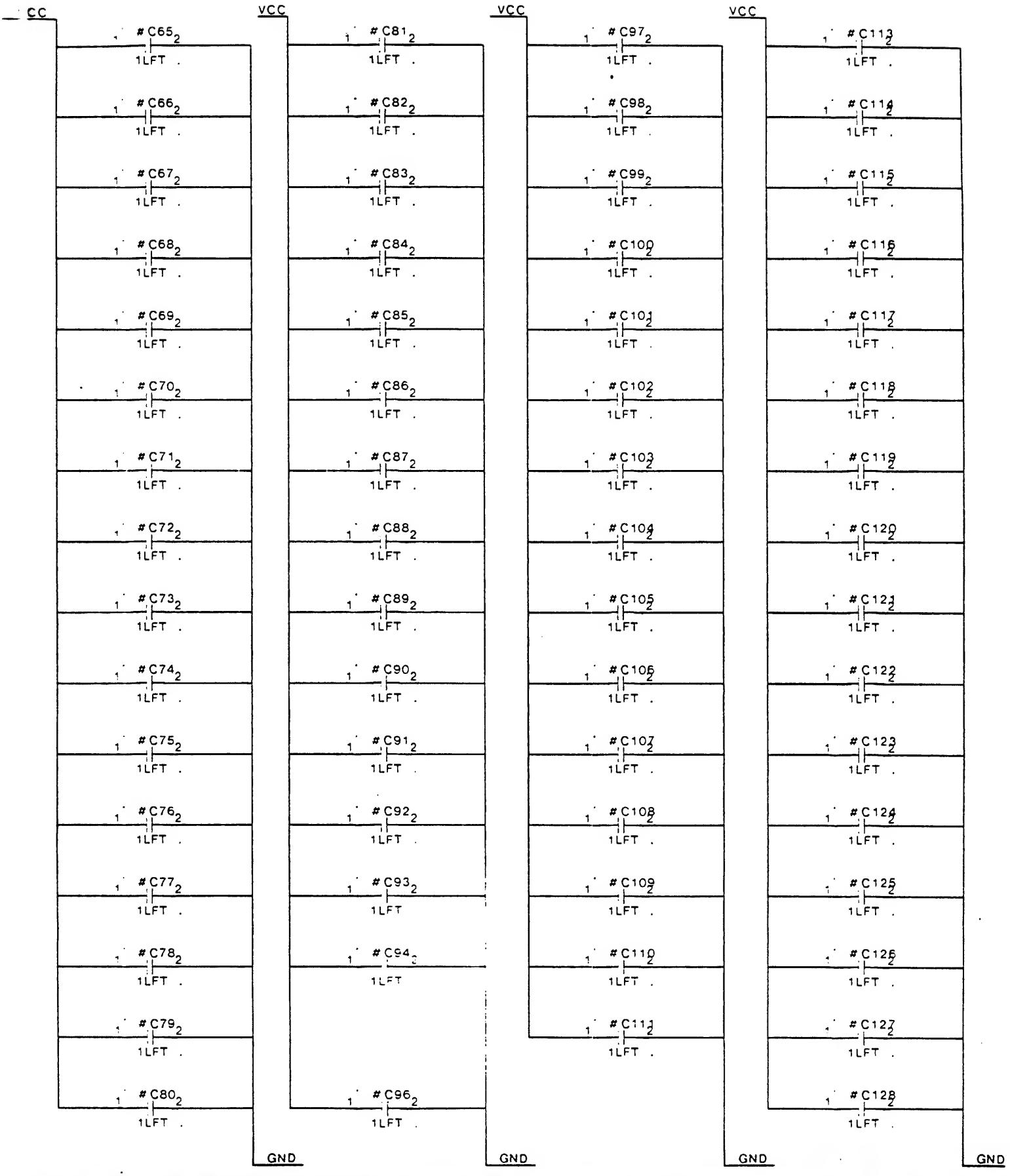
Power Pins - Fuses - Caps

XEROX ED	Project MCCP	Power Pins - Fuses - Caps	File PMCCP34.sil	Designer S. Ando	Rev A	Date 10/17/83	Page 34



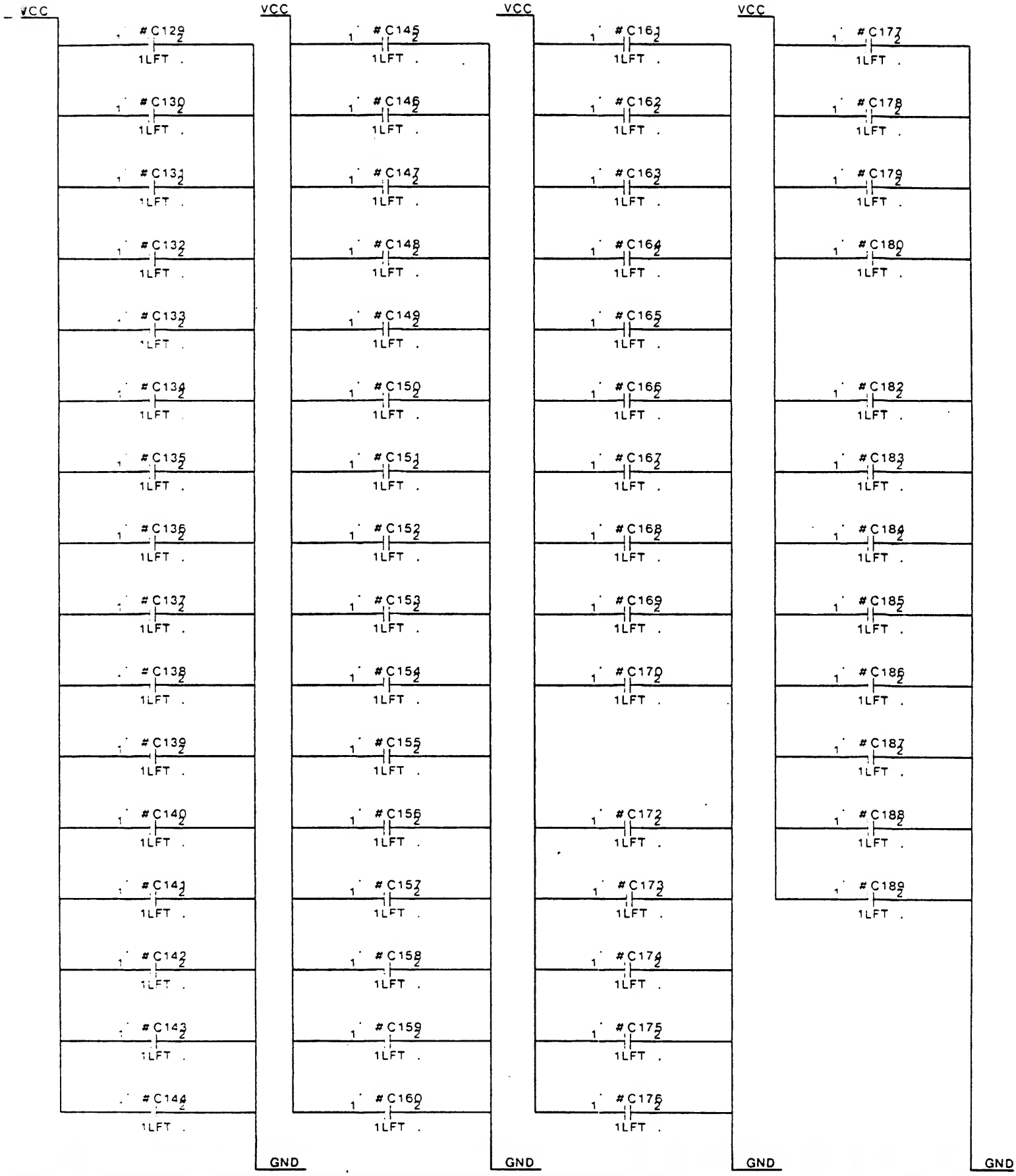
Discrete Capacitors page a

XEROX ED	Project MCCP	Discrete Capacitors	File PMCCP35.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 35



Discrete Capacitors page b

XEROX ED	Project MCCP	Discrete Capacitors	File PMCCP36.sil	Designer S. Ando	Rev A	Date 8/31/83	Page 36



Discrete Capacitors page c

XEROX ED	Project MCCP	Discrete Capacitors	File PMCCP37.sil	Designer S. Ando	Rev A	Date 10/17/83	Page 37